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Contact Information

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Education

Harvard University	Engineering Science	Ph.D. 2010
Tsinghua University	Electrical Engineering	B.S. 2006

Current and Previous Academic Positions:

2019-presnet: Temple Foundation Endowed Associate Professor at the University of Texas at Austin
2017-2019: Tenured Associate Professor at the University of Texas at Austin
2013-2017: AMD Endowed Development Chair at the University of Texas at Austin
2011-2016: Assistant Professor at the University of Texas at Austin

Other Professional Experience

2011-present: Consultant for several top IC design companies
2008-2010: Teaching Assistant at Harvard University
2006-2010: Research Assistant at Harvard University

Honors, Awards, and Recognitions

2019-2020: IEEE Circuits and Systems Society Distinguished Lecturer
2017: Best Student Paper Award at IEEE Custom Integrated Circuits Conference
2016: Nominated for Dean's Award for Outstanding Engineering Teaching
2016: Jack Kilby Research Award from ECE Department, UT Austin
2016: IEEE Senior Membership
2015: Nominated for Dean's Award for Outstanding Engineering Teaching
2015: Jack Kilby Research Award from ECE Department, UT Austin
2014: IEEE Circuits-and-Systems Society Chapter of the Year Award
2013: AMD Endowed Development Chair
2013: NSF CAREER Award
2011: UT Austin Summer Research Assignment Award
2010: Harvard Teaching Award
2009: Harvard Teaching Award
2008: Harvard Teaching Award
2007: Analog Devices Outstanding Student Designer Award
2006: Harvard Graduate Fellowship
2006: Caltech Atwoods Fellowship, Stanford 3-Quarter Fellowship, Yale Fellowship (declined)
2006: Tsinghua University Outstanding Undergraduate Thesis Award
2006: Rank 1/160 at Tsinghua EE Department and Graduate with the Highest Honor
2005: Hewlett-Packard Fellowship
2004: December 9 (12-9) Fellowship
2003: Samsung Fellowship
2003-2005: Tsinghua University First Class Academic Awards for three consecutive times
2003: Top Prize in Intercollegiate Physics Competition

2002: Tsinghua University Freshman Award
2001: 1st-Prize in National Physics Olympiad, Beijing, China
2000: 1st-Prize in National Math Olympiad, Beijing, China

Memberships in Professional and Honorary Societies:
2016-present: Senior Member of Institute of Electrical and Electronics Engineers (IEEE)
2011-2015: Member of IEEE

University Committee Assignments:
Departmental
2016-present: ECE curriculum reform committee
2015-present: ECE colloquium committee
2015-present: ECE junior faculty search committee
2011-present: ECE integrated circuits and systems (ICS) area graduate admission committee
2011-present: ECE ICS area seminar organizer
2014-2015: ECE Silicon Laboratories Endowed Chair search committee
Collegiate:
2012-2014: University Parking and Traffic Appeals Committee

Professional Society Service:
2018-present: Guest Editor for *IEEE Journal of Solid-State Circuits*.
2016-present: Associate Editor for *IEEE Trans. on Circuits and Systems – I, Regular Papers*
2016-present: Associate Editor for *Journal of Semiconductor*
2016-present: Technical program committee member in *IEEE Custom Integrated Circuits Conference*
2012-present: Technical program committee member in *IEEE Asian Solid-State Circuits Conference*
2012-present: Vice Chair of IEEE Central Texas Solid-State-Circuits Society Chapter
2012-present: Vice Chair of IEEE Central Texas Circuits-and-Systems Society Chapter

United States Governmental Committee Service:
2012-present: Proposal review panelist for National Science Foundation (NSF) for 4 times

Published Research Papers
Peer Reviewed Journal Papers:

1. Chen-Kai Hsu, Tim Andeen, and **Nan Sun**, "A Pipeline SAR ADC with Second-order Interstage Gain Error Shaping," *IEEE Journal of Solid-State Circuits*, accepted (VLSI invited submission).
2. Xiyuan Tang, Linxiao Shen, Begum Kasap, Xiangxing Yang, Wei Shi, Abhishek Mukherjee, David Z. Pan, and **Nan Sun**, "An Energy-Efficient Comparator with Dynamic Floating Inverter Amplifier," *IEEE Journal of Solid-State Circuits*, accepted (VLSI invited submission).
3. Wenda Zhao, Shaolan Li, Biying Xu, Xiangxing Yang, Xiyuan Tang, Linxiao Shen, Nanshu Lu, David Z. Pan, and **Nan Sun**, "A 0.025-mm2 0.8-V 78.5dB-SNDR VCO-Based Sensor Readout Circuit in a Hybrid PLL-ΔΣM Structure," *IEEE Journal of Solid-State Circuits*, accepted (CICC invited submission).
4. Yanlong Zhang, Arindam Sanyal, Xueyi Yu, Xing Quang, Kailin Wen, Xiyuan Tang, Gang Jin, Li Geng, and **Nan Sun**, "A Fractional-N PLL With Space-Time Averaging for Quantization Noise Reduction," *IEEE Journal of Solid-State Circuits, accepted* (CICC invited submission).
5. Yi Zhong, Shaolan Li, Xiyuan Tang, Linxiao Shen, Wenda Zhao, Siliang Wu, and **Nan Sun**, "A Second-Order Purely VCO-Based CT ΔΣ ADC Using a Modified DPLL Structure in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, accepted.

6. Yi Shen, Xiyuan Tang, Linxiao Shen, Wenda Zhao, Xin Xin, Shubin Liu, Zhangming Zhu, Visvesh Sathe, and **Nan Sun**, "A 10-bit 120-MS/s SAR ADC with Reference Ripple Cancellation Technique," *IEEE Journal of Solid-State Circuits*, accepted (CICC invited submission).
7. Haoyu Zhuang, Xiaodan Xi, **Nan Sun**, and Michael Orshansky, "A Strong Subthreshold Current Array PUF Resilient to Machine Learning Attacks," *IEEE Transactions on Circuits and Systems - I: Regular Papers*, accepted.
8. Shaolan Li, David Pan, and **Nan Sun**, "An OTA-less Second-Order VCO-based CT ΔΣ Modulator Using an Inherent Passive Integrator and Capacitive Feedback," *IEEE Journal of Solid-State Circuits*, accepted.
9. Linxiao Shen, Yi Shen, Zhelu Li, Wei Shi, Xiyuan Tang, Shaolan Li, Wenda Zhao, Mantian Zhang, Zhangming Zhu, and **Nan Sun**, "A Two-Step ADC with a Continuous-Time SAR Based First Stage," *IEEE Journal of Solid-State Circuits*, accepted.
10. Hyoyoung Jeong, Liu Wang, Taewoo Ha, Ruchika Mitbander, Xiangxing Yang, Zhaohe Dai, Shutao Qiao, Linxiao Shen, **Nan Sun**, Nanshu Lu, "Modular and Reconfigurable Wireless E-Tatoos for Personalized Sensing," *Advanced Materials Technologies*, 2019.
11. Jeonggoo Song, Kareem Ragab, Xiyuan Tang, and **Nan Sun**, "A 10-b 600-MS/s 2-Way Time-Interleaved SAR ADC with Mean Absolute Deviation Based Background Timing-Skew Calibration," *IEEE Transactions on Circuits and Systems - I: Regular Papers*, vol. 66, no. 8, pp. 2876-2887, Aug. 2019.
12. Shaolan Li, Arindam Sanyal, Kyoungtae Lee, Yeonam Yoon, Xiyuan Tang, Yi Zhong, Kareem Ragab, and **Nan Sun**, "Advances in Voltage-Controlled-Oscillator-Based ΔΣ ADCs," *IEICE Transactions on Electronics*, vol. 102, no. 7, page 509-519, July 2019.
13. Haoyu Zhuang, Wenjuan Guo, Jiaxin Liu, He Tang, Zhangming Zhu, Long Chen, and **Nan Sun**, "A Second-Order Noise-Shaping SAR ADC with Passive Integrator and Tri-Level Voting," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1636-1647, June 2019.
14. Jiaxin Liu, Chen-Kai Hsu, Xiyuan Tang, Shaolan Li, Guangjun Wen, and **Nan Sun**, "Error-Feedback Mismatch Error Shaping for High-Resolution Data Converters," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 66, no. 4, pp. 1342-1354, April 2019.
15. David Ricketts, En Shi, Xiaofeng Li, **Nan Sun**, Ozgur Yildirim, Donhee Ham, "Electrical Solitons for Microwave Systems: Harmonizing Nonlinearity and Dispersion with Nonlinear Transmission Line," *IEEE Microwave Magazine*, vol. 20, no. 4, pp. 123-134, Mar. 2019.
16. Jiaxin Liu, Shaolan Li, Wenjuan Guo, Guangjun Wen, and **Nan Sun**, "A 0.029-mm2 17-fJ/Conversion-Step Third-Order CT ΔΣ ADC With a Single OTA and Second-Order Noise-Shaping SAR Quantizer," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 428-440, Feb. 2019.
17. Abhishek Mukherjee, Miguel Gandara, Biying Xu, Shaolan Li, Linxiao Shen, Xiyuan Tang, David Pan, and **Nan Sun**, "A 1 GS/s 20 MHz-BW Capacitive-Input Continuous Time ΔΣ ADC Using a Novel Parasitic Pole-Mitigated Fully Differential VCO," *IEEE Solid-State Circuits Letters*, vol. 2, no. 1, pp. 1-4, Jan. 2019.
18. Dengquan Li, Zhangming Zhu, Ruixue Ding, Maliang Liu, Yintang Yang, and **Nan Sun**, "A 10-bit 600-MS/s Time-Interleaved SAR ADC with Interpolation-Based Timing Skew Calibration," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 66, no. 1, pp. 16-20, Jan. 2019.
19. Shaolan Li, Qiao Bo, Miguel Gandara, David Pan, and **Nan Sun**, "A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure," *IEEE Journal of Solid-State Circuits* (ISSCC invited submission), vol. 53, no. 12, pp. 3484-3496, Dec. 2018.
20. Linxiao Shen, Nanshu Lu, and **Nan Sun**, "A 1-V 0.25-μW Inverter Stacking Amplifier with 1.07 Noise Efficiency Factor," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 896-905, Mar. 2018.

21. Yeonam Yoon and **Nan Sun**, "A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle Code Correction, Resolution Enhancement, and Background Window Width Calibration," *IEEE Journal of Solid-State Circuits* (CICC invited submission), vol. 53, no. 3, pp. 789-798, Mar. 2018.
22. Jiaxin Liu, Guangjun Wen, and **Nan Sun**, "Second-order DAC mismatch error shaping for SAR ADCs," *Electronic Letters*, vol.53, no. 24, pp. 1570-1572, Nov. 2017.
23. Jeonggoo Song, Kareem Ragab, Xiyuan Tang, and **Nan Sun**, "A 10-b 800MS/s Time-Interleaved SAR ADC with Fast Variance-Based Timing-Skew Calibration," *IEEE Journal of Solid-State Circuits* (ASSCC invited submission), vol. 52, no. 10, pp. 2563-2575, Oct. 2017.
24. Wenjuan Guo, Youngchun Kim, Ahmed Tewfik, and **Nan Sun**, "A Fully-Passive Compressive Sensing SAR ADC for Low-Power Wireless Sensors," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2154-2167, Aug. 2017.
25. Shaolan Li, Abhishek Mukherjee, and **Nan Sun**, "A 174.3dB FoM VCO-Based CT ΔΣ Modulator with a Fully Digital Phase Extended Quantizer and Tri-Level Resistor DAC in 130nm CMOS," *IEEE Journal of Solid-State Circuits* (ESSCIRC invited submission), vol. 52, no. 7, pp. 1940-1952, July 2017.
26. Arindam Sanyal and **Nan Sun**, "An Energy-Efficient Hybrid SAR-VCO ΔΣ Capacitance-to-Digital Converter in 40nm CMOS," *IEEE Journal of Solid-State Circuits* (ESSCIRC invited submission), vol. 52, no. 7, pp. 1966-1976, July 2017.
27. Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and **Nan Sun**, "A 0.7V 0.6μW 100kS/s Low-Power SAR ADC with Statistical Estimation Based Noise Reduction," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1388-1398, May 2017.
28. Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and **Nan Sun**, "A 0.95-mW 6-b 700-Ms/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 64, no. 3, pp. 244-248, Mar. 2017.
29. Kareem Ragab and **Nan Sun**, "A 12b ENOB, 2.5MHz, 4.8mW VCO-based 0-1 MASH with direct digital background calibration," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 433-447, Feb. 2017.
30. Arindam Sanyal and **Nan Sun**, "A second-order VCO-based delta sigma ADC using a modified DPLL," *Electronics Letters*, vol. 52, no. 14, pp. 1204-1205, Jun. 2016.
31. Arindam Sanyal, Xueyi Yu, Yanlong Zhang, and **Nan Sun**, "Fractional-N PLL with multi-element fractional divider for noise reduction," *Electronic Letters*, vol. 52, no. 10, pp. 809-810, May 2016.
32. Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A scaling-friendly low-power small-area delta-sigma ADC with VCO-based integrator and intrinsic mismatch shaping capability," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561-573, Dec. 2015.
33. Arindam Sanyal and **Nan Sun**, "Dynamic element matching techniques for static and dynamic errors in continuous-time multi-bit delta-sigma modulators," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 598-611, Dec. 2015.
34. Wenjuan Guo, Tsedeniya Abraham, Steven Chiang, Chintan Trehan, Masahiro Yoshioka, and **Nan Sun**, "An area and power-efficient Iref compensation technique for voltage-mode R-2R DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 7, pp. 656-660, July 2015.
35. Dongwan Ha, **Nan Sun**, and Donhee Ham, "Next generation multidimensional NMR spectrometer based on semiconductor technology," *eMagRes*, vol. 4, pp. 117-125, 2015.
36. Arindam Sanyal, Long Chen, and **Nan Sun**, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 62, no. 5, pp. 1325-1334, May 2015.
37. Manzur Rahman, Arindam Sanyal, and **Nan Sun**, "A novel hybrid radix-3/radix-2 SAR ADC with fast convergence and low hardware complexity," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 5, pp. 426-430, May 2015.
38. Kareem Ragab, Long Chen, Arindam Sanyal, and **Nan Sun**, "Digital background calibration for pipelined ADCs based on comparator decision time quantization," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 62, no. 5, pp. 456-460, May 2015.

39. Dongwan Ha, Jeffrey Paulsen, **Nan Sun**, Yi-Qiao Song, and Donhee Ham, "Scalable NMR spectroscopy with semiconductor chips," *Proceedings of National Academy of Engineering (PNAS)*, vol. 111, no. 33, pp. 11955–11960, Aug. 2014.
40. Arindam Sanyal, Peijun Wang, and **Nan Sun**, "A thermometer-like mismatch shaping technique with minimum element transition activity for multibit delta-sigma DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 61, no. 7, pp. 461-465, Jul. 2014.
41. Arindam Sanyal and **Nan Sun**, "An energy-efficient, low frequency-dependence switching technique for SAR ADCs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 61, no. 5, pp. 294-298, May 2014.
42. Kareem Ragab, Mucahit Kozak, and **Nan Sun**, "Thermal noise analysis of a programmable-gain switched-capacitor amplifier with input offset cancellation," *IEEE Transactions on Circuits and Systems – II, Express Briefs*, vol. 60, no. 3, pp. 147-151, Mar. 2013.
43. **Nan Sun**, Yong Liu, Ling Qin, Hakho Lee, Ralph Weissleder, and Donhee Ham, "Small NMR biomolecular sensors," *Journal of Solid-State Electronics* (invited paper), vol. 84, pp. 13-21, Mar. 2013.
44. Arindam Sanyal and **Nan Sun**, "SAR ADC architecture with 98% reduction in switching energy over conventional scheme," *Electronics Letters*, vol. 49, pp. 248-250, 2013.
45. **Nan Sun**, "Exploiting process variation and noise in comparators to calibrate interstage gain nonlinearity in pipelined ADCs," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 4, pp. 685-695, Apr. 2012.
46. Youngchun Kim, Wenjuan Guo, Vikrham Gowreesunker, **Nan Sun**, and Ahmed Tewfik, "Multi-channel sparse data conversion with a single analog-to-digital converter," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 2, pp. 470-481, Sept. 2012.
47. **Nan Sun**, "High-order mismatch-shaped segmented multibit delta-sigma DACs with arbitrary unit weights," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 59, no. 2, pp. 295-304, Feb. 2012.
48. **Nan Sun** and Peiyan Cao, "Low-complexity high-order vector-based mismatch shaping in multi-bit ΔΣ ADCs," *IEEE Transactions on Circuits and Systems - II: Express Briefs*, vol. 58, no. 12, pp. 872-876, Dec. 2011.
49. **Nan Sun**, "High-order mismatch-shaping in multibit DACs," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 58, no. 6, pp 346-350, Jun. 2011.
50. **Nan Sun**, Tae-Jong Yoon, Hakho Lee, William Andress, Ralph Weissleder, and Donhee Ham, "Palm NMR and one-chip NMR," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 342-352, Jan. 2011.
51. **Nan Sun**, Yong Liu, Hakho Lee, Ralph Weissleder, and Donhee Ham, "CMOS RF biosensor utilizing nuclear magnetic resonance," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1629-1643, May 2009.
52. **Nan Sun**, Hae-Seung Lee, and Donhee Ham, "Digital background calibration in pipelined ADCs using commutated feedback capacitor switching," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 55, no. 9, pp. 877-881, Sept. 2008.
53. **Nan Sun**, William Andress, Kyoungho Woo, and Donhee Ham, "Surpassing tradeoffs by separation: examples in transmission line resonators, phase-locked loops, and analog-to-digital converters," (invited paper) *Journal of Semiconductor Technology and Science*, vol. 8, pp. 210-220, Sept. 2008.
54. David Ricketts, Xiaofeng Li, **Nan Sun**, Kyoungho Woo and Donhee Ham, "On the self-generation of electrical soliton pulses," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1657-1668, August 2007.

Peer Reviewed Conference papers:

1. Haoyu Zhuang, Jiaxin Liu, and **Nan Sun**, "A Fully-Dynamic Time-Interleaved Noise-Shaping SAR ADC Based on CIFF Architecture," *IEEE Custom Integrated Circuits Conference* (CICC), Mar. 2020, accepted.

2. Chen-Kai Hsu, Xiyuan Tang, Wenda Zhao, Rui Xu, Abhishek Mukherjee, Timothy Andeen, **Nan Sun**, "A 77.1-dB 6.25-MHz-BW Pipeline SAR ADC with Enhanced Interstage Gain Error Shaping and Quantization Error Shaping," *IEEE Custom Integrated Circuits Conference* (CICC), Mar. 2020, accepted.
3. Mingjie Liu*, Keren Zhu*, Jiaqi Gu, Linxiao Shen, Xiyuan Tang, **Nan Sun** and David Z. Pan, "Towards Decrypting the Art of Analog Layout, Placement Quality Prediction via Transfer Learning, " *IEEE Design, Automation & Test in Europe Conference & Exhibition* (DATE), Grenoble, France, Mar. 09-13, 2020. (* indicates equal contributions)
4. Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, **Nan Sun** and David Z. Pan, "S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity, " *IEEE/ACM Asian and South Pacific Design Automation Conference* (ASPDAC), Beijing, China, Jan. 13-16, 2020. (Best Paper Award Nomination)
5. Jiaxin Liu, Xiyuan Tang, Wenda Zhao, Linxiao Shen, and **Nan Sun**, "A 13-bit 0.005mm^2 40MS/s SAR ADC with kT/C Noise Cancellation," *IEEE International Solid-State Circuits Conference* (ISSCC), 2020, to appear.
6. Jiaxin Liu, Xing Wang, Zijie Gao, Mingtao Zhan, Xiyuan Tang, and **Nan Sun**, "A 40kHz-BW 90dB-SNDR Noise-Shaping SAR with 4× Passive Gain and 2nd-order Mismatch Error Shaping," *IEEE International Solid-State Circuits Conference* (ISSCC), 2020, to appear.
7. Xiyuan Tang, Xiangxing Yang, Wenda Zhao, Chen-Kai Hsu, Jiaxin Liu, Linxiao Shen, Abhishek Mukherjee, Wei Shi, David Pan, and **Nan Sun**, "A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier," *IEEE International Solid-State Circuits Conference* (ISSCC), 2020, to appear.
8. Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, **Nan Sun,** and David Z. Pan, "S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity, " *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Beijing, China, Jan. 13-16, 2020, to appear.
9. Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, **Nan Sun,** and David Z. Pan, "GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance, " *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019, to appear.
10. Xiyuan Tang, Begum Kasap, Linxiao Shen, Xiangxing Yang, Wei Shi, and **Nan Sun**, "An Energy-Efficient Comparator with Dynamic Floating Inverter Pre-Amplifier," *IEEE Symposium on VLSI Circuits* (VLSI), June 2019, C140-C141.
11. Linxiao Shen, Abhishek Mukherjee, Shaolan Li, Xiyuan Tang, Nanshu Lu, and **Nan Sun**, "A 0.6-V Tail-Less Inverter Stacking Amplifier with 0.96 PEF," *IEEE Symposium on VLSI Circuits* (VLSI), June 2019, C144-C145.
12. Chen-Kai Hsu and **Nan Sun**, "A 75.8dB-SNDR Pipeline SAR ADC with 2nd-order Interstage Gain Error Shaping," *IEEE Symposium on VLSI Circuits* (VLSI), June 2019, C68-C69.
13. Biying Xu, Yibo Lin, Xiyuan Tang, Shaolan Li, Linxiao Shen, **Nan Sun** and David Z. Pan, "WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.
14. Biying Xu, Shaolan Li, Chak-Wa Pui, Derong Liu, Linxiao Shen, Yobo Lin, **Nan Sun** and David Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits," *IEEE International Symposium on Physical Design* (ISPD), 2019.
15. Yanlong Zhang, Arindam Sanyal, Xing Quan, Kailin Wen, Xiyuan Tang, Gang Jin, Li Geng and **Nan Sun**, "A 2.4-GHz ΔΣ Fractional-N Synthesizer with Space-Time Averaging for Noise Reduction," *IEEE Custom Integrated Circuits Conference* (CICC), April 2019.
16. Shaolan Li, Wenda Zhao, Biying Xu, Xiangxing Yang, Xiyuan Tang, Linxiao Shen, Nanshu Lu, David Pan and **Nan Sun**, "A 0.025-mm2 0.8-V 78.5dB-SNDR VCO-based Sensor Readout Circuit in a Hybrid PLL-ΔΣM Structure," *IEEE Custom Integrated Circuits Conference* (CICC), April 2019.

17. Dengquan Li, Jiaxin Liu, Haoyu Zhuang, Zhangming Zhu, Yintang Yang and **Nan Sun**, "A 7b 2.6mW 900MS/s Nonbinary 2-then-3b/cycle SAR ADC with Background Offset Calibration," *IEEE Custom Integrated Circuits Conference* (CICC), April 2019.
18. Xiyuan Tang, Yi Shen, Linxiao Shen, Wenda Zhao, Zhangming Zhu, Visvesh Sathe and **Nan Sun**, "A 10b 120MS/s SAR ADC with Reference Ripple Cancellation Technique," *IEEE Custom Integrated Circuits Conference* (CICC), April 2019.
19. Shaolan Li, Biying Xu, David Pan and **Nan Sun**, "A 60-fJ/step 11-ENOB VCO-based CTDSM Synthesized from Digital Standard Cell Library," *IEEE Custom Integrated Circuits Conference* (CICC), April 2019.
20. Linxiao Shen, Yi Shen, Xiyuan Tang, Chen-Kai Hsu, Wei Shi, Shaolan Li, Wenda Zhao, and **Nan Sun**, "A 0.01mm^2 25uW 2MS/s 74dB-SNDR Continuous-Time Pipelined-SAR ADC with 120fF Input Capacitor," *IEEE international Solid-State Circuits Conference* (ISSCC), 2019, pp. 64-66.
21. Xiyuan Tang, Shaolan Li, Linxiao Shen, Wenda Zhao, Xiangxing Yang, Randy Williams, Jiaxin Liu, Zhichao Tan, Neal Hall, **Nan Sun**, "A 16fJ/conversion-step Time-Domain Incremental Zoom Capacitance-to-Digital Converter," *IEEE International Solid-State Circuits Conference* (ISSCC), 2019, pp. 296-297.
22. Yi Zhong, Shaolan Li, Arindam Sanyal, Xiyuan Tang, Linxiao Shen, Siliang Wu, **Nan Sun**, "A Second-Order Purely VCO-Based CT $\Delta\Sigma$ ADC Using a Modified DPLL in 40-nm CMOS," *IEEE Asian Solid-State Circuits Conference* (ASSCC), Nov. 2018, pp. 93-94.
23. Jiaxin Liu, Shaolan Li, Wenjuan Guo, Guangjun Wen and **Nan Sun**, "A 0.029mm^2 17-fJ/Conv.-Step CT Delta-Sigma ADC with 2nd-Order Noise-Shaping SAR Quantizer," *IEEE Symposium on VLSI Circuits*, June 2018, pp. 201-202.
24. Arindam Sanyal, Shaolan Li, and **Nan Sun**, "Low-power Scaling-friendly Ring Oscillator based Delta-Sigma ADC," *IEEE International Symposium on Circuits and Systems* (invited), May 2018, pp. 1-5.
25. Jeonggoo Song and **Nan Sun**, "A 10-b 600-MS/s 2-Way Time-Interleaved SAR ADC with Mean Absolute Deviation Based Background Timing-Skew Calibration," *IEEE Custom Integrated Circuits Conference* (CICC), May 2018, pp. 1-4.
26. Shaolan Li, Bo Qiao, Miguel Gandara, and **Nan Sun**, "A 13-bit ENOB 2nd-order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure," *IEEE International Solid-State Circuits Conference* (*ISSCC*), Feb. 2018, pp. 234 - 236.
27. Miguel Gandara, Paridhi Gulati, and **Nan Sun**, "A 172dB-FoM Pipelined SAR ADC Using a Regenerative Amplifier with Self-Timed Gain Control and Mixed-Signal Background Calibration," *IEEE Asian Solid-State Circuits Conference* (ASSCC), Nov. 2017, pp. 297-300.
28. Xiyuan Tang, Long Chen, Jeonggoo Song, and **Nan Sun**, "A 1.5fJ/Conv-step 10b 100kS/s SAR ADC with Power-Efficient Noise Reduction," *IEEE Asian Solid-State Circuits Conference* (ASSCC), Nov. 2017, pp. 229-232.
29. Dongwan Ha, **Nan Sun**, Jeffrey Paulsen, Yiqiao Song, and Donhee Ham, "Integrated CMOS Spectrometer for Multi-Dimensional NMR Spectroscopy," *IEEE Midwest Symposium on Circuits and Systems* (invited), Aug. 2017, pp. 1085-1088.
30. Hyoyoung Jeong, Taewoo Ha, Irene Kuang, Linxiao Shen, Zhaohe Dai, **Nan Sun**, Nanshu Lu, "NFC-Enabled, Tattoo-Like Stretchable Biosensor Manufactured by "Cut-and-Paste" Method," *39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society* (EMBC), July 2017, pp. 4094-4097.
31. Linxiao Shen, Nanshu Lu, and **Nan Sun**, "A 1V 0.25uW Inverter-Stacking Amplifier with 1.07 Noise Efficiency Factor," *IEEE Symposium on VLSI Circuits*, pp. C140-C141, June 2017.
32. Shaolan Li and **Nan Sun**, "A 0.028mm2 19.8fJ/step 2nd-Order VCO-based CT Delta Sigma Modulator Using an Inherent Passive Integrator and Capacitive Feedback in 40nm CMOS," *IEEE Symposium on VLSI Circuits*, pp. C36-C37, June 2017.
33. Wenjuan Guo, Haoyu Zhuang, and **Nan Sun**, "A 13b-ENOB 173dB-FoM 2nd -Order NS SAR ADC with Passive Integrators," *IEEE Symposium on VLSI Circuits*, pp. C236-C237, June 2017.

34. Xiaodan Xi, Haoyu Zhuang, **Nan Sun**, and Michael Orshansky, "Strong Subthreshold Current Array PUF with 2^65 Challenge-Response Pairs Resilient to Machine Learning Attacks in 130nm CMOS," *IEEE Symposium on VLSI Circuits*, pp. C268-C269, June 2017.
35. Biying Xu, Shaolan Li, **Nan Sun**, and David Z. Pan, "A Scaling Compatible, Synthesis Friendly VCO-based Delta-sigma ADC Design and Synthesis Methodology," *IEEE Design Automation Conference* (DAC), 2017.
36. Biying Xu, Shaolan Li, Xiaoqing Xu, **Nan Sun**, and David Z. Pan, "Hierarchical and Analytical Placement Techniques for High-Performance Analog Circuits," *IEEE International Symposium on Physical Design* (ISPD), 2017.
37. Yeonam Yoon and **Nan Sun**, "A 6-bit 0.81mW 700-MS/s SAR ADC with Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration," *IEEE Custom Integrated Circuits Conference* (CICC), May 2017.
38. Miguel Gandara, Wenjuan Guo, Xiyuan Tang, Long Chen, Yeonam Yoon, and **Nan Sun**, "A Pipelined SAR ADC Reusing the Comparator as Residue Amplifier," *IEEE Custom Integrated Circuits Conference* (CICC), May 2017.
39. Jeonggoo Song, Xiyuan Tang, and **Nan Sun**, "A 10-b 2b/cycle 300MS/s SAR ADC with a Single Differential DAC in 40nm CMOS," *IEEE Custom Integrated Circuits Conference* (CICC), May 2017.
40. Jeonggoo Song, Kareem Ragab, Xiyuan Tang, and **Nan Sun**, "A 10-b 800MS/s time-interleaved SAR ADC with fast timing-skew calibration," *IEEE Asian Solid-State Circuits Conference (ASSCC)*, pp. 73-76, Nov. 2016.
41. Wenjuan Guo and **Nan Sun**, "A 9.8b-ENOB 5.5fJ/step fully-passive compressive sensing SAR ADC for WSN applications," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 91-94, Sept. 2016.
42. Shaolan Li and **Nan Sun**, "A 174.3dB FoM VCO-based CT ΔΣ modulator with a fully digital phase extended quantizer and tri-level resistor DAC in 130nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 241-244, Sept. 2016.
43. Kareem Ragab and **Nan Sun**, "A 1.4mW 8b 350MS/s loop-unrolled SAR ADC with background offset calibration in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 417-420, Sept. 2016.
44. Arindam Sanyal and **Nan Sun**, "A 55fJ/conv-step hybrid SAR-VCO delta sigma capacitance-to-digital converter in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 385-388, Sept. 2016.
45. Xiyuan Tang, Long Chen, Jeonggoo Song, and **Nan Sun**, "A 10-b 750μW 200MS/s fully dynamic single-channel SAR ADC in 40nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 413-416, Sept. 2016.
46. Wenjuan Guo and **Nan Sun**, "A 12b-ENOB 61μW noise-shaping SAR ADC with a passive integrator," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 405-408, Sept. 2016.
47. Arindam Sanyal and **Nan Sun**, "A 18.5-fJ/step VCO-based 0-1 MASH delta-sigma ADC with digital background calibration," *IEEE Symposium on VLSI Circuits*, pp. 26-27, Jun. 2016.
48. Long Chen, Arindam Sanyal, Ji Ma, Xiyuan Tang, and **Nan Sun,** "Comparator common-mode variation effects analysis and its application in SAR ADCs," *IEEE International Symposium on Circuits and Systems*, pp. 2014-2017, May 2016.
49. Wenjuan Guo, Youngchun Kim, Ahmed Tewfik, and **Nan Sun**, "Ultra-low power multi-channel data conversion with a single SAR ADC for mobile sensing applications", *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.
50. Yeonam Yoon, Koungtae Lee, Sungjin Hong, Xiyuan Tang, Long Chen, and **Nan Sun**, "A 0.04-mm2 0.9-mW 71-dB SNDR distributed modular ΔΣ ADC with VCO-based integrator and digital DAC calibration," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.
51. Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and **Nan Sun**, "A 10.5-b ENOB 645nW 100kS/s SAR ADC with statistical estimation based noise reduction," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.

52. Kareem Ragab and **Nan Sun**, "A 12b ENOB, 2.5MHz-BW, 4.8mW VCO-based 0-1 MASH ADC with direct digital background nonlinearity calibration," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2015.
53. Arindam Sanyal, Kareem Ragab, Long Chen, T.R. Viswanathan, Shouli Yan, and **Nan Sun**, "A hybrid SAR-VCO delta-sigma ADC with first-order noise shaping," *Custom Integrated Circuit Conference (CICC)*, pp. 1-4, Sept. 2014.
54. Long Chen, Arindam Sanyal, Ji Ma, and **Nan Sun**, "A 24-uW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique," *European Solid-State Circuit Conference (ESSCIRC)*, pp. 219-222, Sept. 2014.
55. Nicholas Wood and **Nan Sun**, "Predicting ADC - a new approach to low power ADC design," *IEEE Dallas Circuits and Systems Conference (DCAS)*, pp. 1-4, Oct. 2014.
56. K. R. Raghunandan, **Nan Sun**, and T.R. Viswanathan, "Analog signal processing in deep submicron CMOS technologies using inverters," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 394-397, Aug. 2014.
57. Arindam Sanyal and **Nan Sun**, "A low frequency-dependence, energy-efficient switching technique for bottom-plate sampled SAR ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 297-300, June 2014.
58. Xiankun Jin and **Nan Sun**, "Low-cost high-quality constant offset injection for SEIR-based ADC built-in-self-test," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 285-288, June 2014.
59. Peijun Wang and **Nan Sun**, "A random DEM technique with minimal element transition rate for high-speed DACs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1155-1158, June 2014.
60. Long Chen, Ji Ma, and **Nan Sun**, "Capacitor mismatch calibration for SAR ADCs based on comparator metastability detection," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2357-2360, June 2014.
61. Arindam Sanyal and **Nan Sun**, "An enhanced ISI shaping technique for multi-bit delta sigma DACs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2341-2344, June 2014.
62. Yeonam Yoon, Kyoungtae Lee, Peijun Wang, and **Nan Sun**, "A purely-VCO-based single-loop high-order continuous-time delta sigma ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 926-929, June 2014.
63. Manzur Rahman, Long Chen, and **Nan Sun**, "Algorithm and implementation of digital calibration of fast converging radix-3 SAR ADC," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1336-1339, June 2014.
64. Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A 1.8mW 2MHz-BW 66.5dB-SNDR delta-sigma ADC using VCO-based integrators with intrinsic CLA," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, Sept. 2013.
65. Arindam Sanyal and **Nan Sun**, "A very high energy-efficiency switching technique for SAR ADCs," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 229-232, Aug. 2013.
66. Rohit Yadav and **Nan Sun**, "A 1.2mW 67.5 dB SQDR VCO-based sigma delta ADC with non-linearity cancellation technique," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 570-573, Aug. 2013.
67. Long Chen, Manzur Rahman, Sha Liu, and **Nan Sun**, "A fast radix-3 SAR analog-to-digital converter," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1148-1151, Aug. 2013.
68. Kyoungtae Lee, Yeonam Yoon, and **Nan Sun**, "A 10MHz-BW, 5.6mW, 70dB SNDR delta-sigma ADC using VCO-based integrators with intrinsic DEM," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2006-2009, May 2013.
69. Wenjuan Guo, Youngchun Kim, Arindam Sanyal, Ahmed Tewfik, and **Nan Sun**, "A single SAR ADC converting multi-channel sparse signals," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2235-2238, May 2013.

70. Travis Forbes, Wei-Gi Ho, **Nan Sun**, and Ranjit Gharpurey, "A frequency-folded ADC architecture with digital LO synthesis," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 149-152, May 2013.
71. **Nan Sun**, Yong Liu, Ling Qin, Guangyu Xu, and Donhee Ham, "Solid-state and biological systems interface," *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*, pp. 14-17, Sept. 2012.
72. **Nan Sun**, Hae-Seung Lee, and Donhee Ham, "A 2.9-mW 11-b 20-MS/s pipelined ADC with dual-mode-based digital background calibration," *Proceedings of European Solid-State Circuit Conference (ESSCIRC)*, pp. 269-272, Sept. 2012.
73. Arindam Sanyal and **Nan Sun**, "A simple and efficient dithering method for vector quantizer based mismatch-shaped ΔΣ DACs," *IEEE Proceedings of International Symposium on Circuits and Systems*, pp. 528 - 531, May 2012.
74. **Nan Sun**, Yong Liu, Hakho Lee, Ralph Weissleder, and Donhee Ham, "Silicon RF NMR biomolecular sensor – Review, " (invited paper) *IEEE Proceedings of International Symposium on VLSI Design, Automation & Test (VLSI-DAT)*, pp. 121-124, Apr. 2010.
75. **Nan Sun**, Tae-Jong Yoon, Hakho Lee, William Andress, Vasiliki Demas, Pablo Prado, Ralph Weissleder, and Donhee Ham, "Palm NMR and one-chip NMR," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 6-8, Feb. 2010.
76. Yong Liu, **Nan Sun**, Hakho Lee, Ralph Weissleder, and Donhee Ham, "CMOS mini nuclear magnetic resonance system and its application for biomolecular sensing, " *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 140-141, Feb. 2008.

Book Chapters

1. Shaolan Li and **Nan Sun**, "Noise-shaping SAR ADCs," invited book chapter in *Advances in Analog Circuit Design*, Springer, 2019, invited.
2. Ka-Meng Lei, **Nan Sun**, Pui-In Mak, Rui Paulo Martins, and Donhee Ham, "Micro-NMR on CMOS for Biomolecular Sensing," invited book chapter in *CMOS Circuits for Biological Sensing and Processing*, Springer, 2018.
3. Arindam Sanyal, Wenjuan Guo, and **Nan Sun**, "Hybrid VCO Based 0-1 MASH and Hybrid ΔΣ SAR," invited book chapter in *Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design*, Springer, 2018.
4. **Nan Sun** and Donhee Ham, "Chapter 6: Hardware Developments, Handheld NMR systems for biomolecular sensing," invited book chapter in *Mobile NMR and MRI*, Royal Society of Chemistry (Edited by Michael Johns), pp. 158-182, 2015.
5. **Nan Sun** and Donhee Ham, "Handheld NMR systems and their applications for biomolecular sensing," invited book chapter in *Point of Care Diagnostics on a Chip*, Springer (Edited by Robert Westervelt and David Issadore), pp. 177-196, 2012.
6. Ozgur Yildirim, **Nan Sun**, and Xiaofeng Li, "Chaotic soliton oscillator and communications," invited book chapter in *Electrical Solitons: Theory, Design, and Applications*, CRC press, pp. 197-208, 2012.
7. **Nan Sun**, Yong Liu, and Donhee Ham, "Low cost diagnostics − RF designer's approach," invited book chapter in *CMOS Biosystems: Where Electronics Meets Biology*, Wiley (Edited by Kris Iniewski), pp. 1629-1643, 2011.

Patents

1. **Nan Sun**, Yong Liu, Hakho Lee, Ralph Weisselder, and Donhee Ham, "Miniaturized magnetic resonance systems and methods," US patent application number 12/681,303.
2. **Nan Sun** and Donhee Ham, "Systems and methods for design and construction of NMR transceiver circuits," US patent application number 12/919,215.
3. **Nan Sun**, "Dual-mode-based digital background calibration for gain variations and device mismatches," US patent application number 12/649,274.

4. Long Chen, Xiyuan Tang, and **Nan Sun**, "Statistical estimation based noise reduction technique for low power successive approximation register analog-to-digital converter," US patent application number 15/278,519.
5. Miguel Gandara and **Nan Sun**, "Variable gain amplifier utilizing positive feedback and time-domain calibration," US patent application number 62/416,805.
6. **Nan Sun**, "Fractional-N phase lock loop apparatus and method using multi-element fractional dividers," US patent application number 16/084,997.
7. Linxiao Shen and **Nan Sun**, "Inverter stacking amplifier," US application number 62/514,684 (pending).

Invited Talks and Seminars:

1. **Nan Sun**, "Energy-Efficient Comparator and Amplifier Design," Cirrus Logic, TX, 8/2019.
2. **Nan Sun**, "Energy-Efficient Comparator and Amplifier Design," Silab, TX, 8/2019.
3. **Nan Sun**, "Advanced ADC Design Techniques," HKUST, Hong Kong, 8/2019.
4. **Nan Sun**, "Advanced ADC Design Techniques," IME, Singapore, 7/2019.
5. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Kobe University, Japan, 6/2019.
6. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Tokyo Institute of Technology, Japan, 6/2019.
7. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," MediaTek, Boston, 4/2019.
8. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Analog Devices, Boston, 4/2019.
9. **Nan Sun**, "When SAR Meets Delta Sigma – A Tale of Two ADC Architectures," 1st ICAC, Chengdu, China, 4/2019.
10. **Nan Sun,** "Handheld CMOS NMR biosensor," Carlos III University, Madrid, Spain, 4/2019.
11. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Polytechnic University of Milan, Italy, 3/2019.
12. **Nan Sun**, "When SAR Meets Delta Sigma – A Tale of Two ADC Architectures." AACD workshop, Milan, Italy, 4/2019.
13. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," TU Delft, Netherland, 3/2019.
14. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Dialog Semiconductor, Netherland, 3/2019.
15. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," IMEC, Belgium, 3/2019.
16. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," KU Leuven, Belgium, 3/2019.
17. **Nan Sun**, "Advanced ADC design," Advanced CMOS technology school, Shenzhen, China, 1/2019.
18. **Nan Sun**, "Recent advanced in analog IC design," IMECAS, Beijing, China, 1/2019.
19. **Nan Sun**, "Recent advanced in analog IC design," Tsinghua University EE Dept. Professor Salon, Beijing, China, 12/2018.
20. **Nan Sun**, "When SAR Meets Delta Sigma – A Tale of Two ADC Architectures." University of Macau, Macau, China, 12/2018.
21. **Nan Sun**, "Recent advances in data conversion techniques," RealTek, Hsinchu, 11/2018.
22. **Nan Sun**, "When SAR Meets Delta Sigma: Hybridization of SAR and Delta Sigma ADCs," AIoT Workshop, National Jiaotong University, Hsinchu, 11/2018.
23. **Nan Sun**, "When SAR Meets Delta Sigma – A Tale of Two ADC Architectures," invited tutorial at ASSCC, Tainan, 11/2018.
24. **Nan Sun**, "When SAR Meets Delta Sigma: Hybridization of SAR and Delta Sigma ADCs," Silabs, TX, 10/2018.

25. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Shanghai Jiaotong University, China, 8/2018.
26. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Fudan University, China, 8/2018.
27. **Nan Sun**, "Hybrid ADCs: Practical Design Considerations and Examples," invited tutorial at ISCAS, Florence, Italy, 5/2018.
28. **Nan Sun**, "When SAR Meets Delta Sigma: Hybridization of SAR and Delta Sigma ADCs," Cirrus Logic, TX, 5/2018.
29. **Nan Sun**, "Analog signal processing – compressive sensing and analog-to-information conversion," Tsinghua University, China, 1/2018.
30. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," UESTC, China, 12/2017.
31. **Nan Sun**, "Advanced ADC design techniques," HKUST, Hong Kong, 12/2017.
32. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," SUSTC, China, 12/2017.
33. **Nan Sun**, "Advanced ADC design techniques," Tsinghua University, China, 11/2017.
34. **Nan Sun**, "Advanced analog IC design techniques," Analog Devices, MA, 10/2017.
35. **Nan Sun**, "Advanced ADC design techniques," Cirrus Logic, TX, 8/2017.
36. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Yonsei University, Korea, 7/2017.
37. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," NPU, China, 7/2017.
38. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Xidian University, China, 7/2017.
39. **Nan Sun**, "Advanced analog circuit design techniques," Tsinghua University, China, 7/2017.
40. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," UESTC, China, 7/2017.
41. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," U. Macau, Macau, 6/2017.
42. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," HKUST, Hong Kong, 6/2017.
43. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Texas Instruments, TX, 5/2017.
44. **Nan Sun**, "Emerging ADC architectures," IEEE CICC ADC Forum, Austin, TX, 5/2017.
45. **Nan Sun**, "Hybrid ADC architectures," AACD workshop, Eindhoven, Netherland, 3/2017.
46. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Gatech, GA, 3/2017.
47. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," University of California at San Diego, CA, 1/2017.
48. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Texas A&M University, TX, 11/2016.
49. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Tsinghua University, China, 11/2016.
50. **Nan Sun,** "Artificial intelligence and analog circuits," IEEE ASSCC Forum, Hakodate, Japan, 11/2016.
51. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," University of Michigan, MI, 10/2016.
52. **Nan Sun**, "New ingredients in the pot – rethink analog IC design," Cirrus Logic, TX, 6/2016.
53. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Stanford University, CA, 5/2016.
54. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Intel Labs, OR, 5/2016.
55. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Oregon State University, Corvallis, OR, 5/2016.
56. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," University of Southern California, Los Angeles, CA, 4/2016.
57. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," University of California at Los Angeles, Los Angeles, CA, 4/2016.

58. **Nan Sun,** "New ingredients in the pot – rethink analog IC design," Broadcom Ltd, Irvine, CA, 4/2016.
59. **Nan Sun,** "Low power analog and mixed-signal IC design for bio-signal detection," BioWireless, Austin, TX, 1/2016.
60. **Nan Sun,** "Advanced analog IC design techniques," Tsinghua University, Beijing, China, 11/2015.
61. **Nan Sun,** "Advanced dynamic element matching techniques for both static and dynamic errors in CT ΔΣ modulator," Cirrus Logic, TX, 6/2015.
62. **Nan Sun,** "Handheld CMOS NMR biosensor," Case Western Reserve University, Cleveland, OH, 4/2015.
63. **Nan Sun,** "Scaling-friendly VCO-based ΔΣ ADC design in advanced CMOS processes," Texas A&M University, College Station, TX, 4/2015.
64. **Nan Sun,** "Low power SAR ADC and high-speed background timing skew calibration," Silicon Labs, Austin, TX, 10/2014.
65. **Nan Sun,** "High performance SAR ADC design," Beijing Microelectronic Technology Institute, 8/2014.
66. **Nan Sun,** "Low-power SAR ADC design," Cirrus Logic, Austin, TX, 6/2014.
67. **Nan Sun,** "Advanced analog IC research," TSMC, Austin, TX, 5/2014.
68. **Nan Sun,** "Handheld CMOS NMR biosensor," Texas Tech University, Lubbock, TX, 11/2013.
69. **Nan Sun,** "Scaling-friendly VCO-based ΔΣ ADC design in advanced CMOS processes," Cirrus Logic, Austin, TX, 11/2013.
70. **Nan Sun,** "Scaling-friendly VCO-based ΔΣ ADC design in advanced CMOS processes," Freescale, AZ, 9/2013.
71. **Nan Sun,** "Handheld CMOS NMR biosensor," Texas Instruments at Santa Clara, CA, 7/2013.
72. **Nan Sun,** "Handheld CMOS NMR biosensor," Kilby Lab, Texas Instruments, TX, 7/2013.
73. **Nan Sun,** "Handheld CMOS NMR biosensor," Texas Instruments, TX, 1/2013.
74. **Nan Sun,** "Mismatch shaping techniques for multibit ΔΣ ADCs," Cirrus Logic, Austin, TX, 1/2013.
75. **Nan Sun,** "Handheld CMOS NMR biosensor," Samsung Research, Dallas, TX, 12/2012.
76. **Nan Sun,** "Advanced dynamic element matching techniques," Synaptics, Austin, TX, 12/2012.
77. **Nan Sun,** "Advanced dynamic element matching techniques," Texas Instruments, TX, 11/2012.
78. **Nan Sun,** "Handheld CMOS NMR biosensor," IEEE Instrumentation and Measurement Chapter, Austin, TX, 05/21/2012.
79. **Nan Sun,** "Handheld CMOS NMR biosensor," Qualcomm, San Diego, CA, 04/13/2012.
80. **Nan Sun,** "Handheld CMOS NMR biosensor," Intel, Portland, OR, 02/17/2012.
81. **Nan Sun,** "Handheld CMOS NMR biosensor," Peking University, Beijing, China, 01/05/2012.
82. **Nan Sun,** "Handheld CMOS NMR biosensor," RWTH Aachen University, Aachen, Germany, 12/13/2011.
83. **Nan Sun,** "Handheld CMOS NMR biosensor," University of Texas at Dallas, Dallas, TX, 11/11/2011.
84. **Nan Sun,** "Handheld CMOS NMR biosensor," IEEE SSCS/CAS Austin Chapter, Austin, TX, 11/02/2011.
85. **Nan Sun,** "Handheld CMOS NMR biosensor," Silicon Labs, Austin, TX, 09/16/2011.
86. **Nan Sun,** "Handheld CMOS NMR biosensor," ICMRM 11, Beijing, China, 08/16/2011.
87. **Nan Sun,** "Handheld CMOS NMR systems," Halliburton, Houston, TX, 06/24/2011.
88. **Nan Sun,** "Advanced dynamic element matching techniques," Tsinghua University, Beijing, China, 01/04/2011.
89. **Nan Sun,** "Handheld CMOS NMR biosensor," IBM T. J. Watson Research Center, Yorktown Heights, NY, 12/10/2010.
90. **Nan Sun,** "Handheld CMOS NMR biosensor," Bruker Biospin Inc., Billerica, MA, 11/16/2010.
91. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, 07/09/2010.

92. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Tsinghua University, Beijing, China, 07/05/2010.
93. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Institute of Electronics, Chinese Academy of Sciences, Beijing, China, 07/01/2010.
94. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Fudan University, Shanghai, China, 06/17/2010.
95. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Shanghai Jiaotong University, Shanghai, China, 06/17/2010.
96. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Rice University, Houston, TX, 04/14/2010.
97. **Nan Sun,** "CMOS RF NMR biosensor & dual-mode pipelined ADC," Stanford University, Stanford, CA, 04/08/2010.
98. **Nan Sun,** "Handheld CMOS NMR biosensor," University of Texas at Austin, Austin, TX, 03/25/2010.
99. **Nan Sun,** "Handheld CMOS NMR biosensor," Harvard University, Cambridge, MA, 03/22/2010.
100. **Nan Sun,** "Handheld CMOS NMR biosensor," Schlumberger-Doll Research Center, Cambridge, MA, 03/10/2010.
101. **Nan Sun,** "Handheld CMOS NMR biosensor," Stanford University, Stanford, CA, 02/04/2010.
102. **Nan Sun,** "CMOS NMR biosensor," Harvard University, 02/02/2010.
103. **Nan Sun,** "CMOS NMR biosensor," CMOS Emerging Technology Conference, Calgary, Canada, 02/2009.

Grants and Contracts (Total ≈ $7M)

Co-Investigators	Title	Agency	Project Total	Grant Period
PI: Nan Sun	Sampling Rate Adaptive ADC Design	Sandia National Lab	$180K	2019-2021
PI: David Pan co-PI: Nan Sun	MAGICAL: Machine Generated Analog IC Layout	DARPA	$1.8M	2018-2022
PI: Nan Sun	Radiation Tolerant Low-Power ADC Design	NSF	$240K	2016-2020
PI: Nan Sun Bo Liu (co-PI) David Pan (co-PI)	SHF: Medium: Integrating Human and Machine Intelligence for Next Generation Interactive Analog IC Design	NSF	$800K	2017-2021
PI: Nan Sun	Ultra-low-power compressive sensing techniques for IoT applications	SRC	$255K	2017-2020
PI: Nan Sun David Pan (co-PI)	SHF: Small: Design/Automation for Synthesizable and Scaling Friendly Analog/Mixed-Signal Circuits	NSF	$450K	2015-2018
PI: Nanshu Lu (Aerospace); co-PI: Nan Sun	Stretchable Planar Antenna Modulated by Integrated Circuit (SPAMIC) for the Near Field Communication (NFC) of Epidermal Electrophysiological Sensors (EEPS)	NSF	$380K	2015-2018
Sub-award PI: Nanshu Lu (Aerospace); Sub-award co-PI: Nan Sun; PI: Katherine	Ubiquitous rehabilitation to monitor and improve muscle activity and movement after neurologic injury	NIH	$1.5M	2015-2019

Steele (University of Washington)				
PI: Nan Sun	CAREER: Combining nuclear magnetic resonance with IC technology	NSF	$400K	2013-2018
PI: Nan Sun	High temperature LNA design	China Oil-Service Ltd	$75K	2015
PI: Nan Sun	Low-power high-speed ADC for CMOS image sensor	Samsung	$100K	2015
PI: Nan Sun	Multichannel MRI transceiver design	Samsung	$100K	2014
PI: Nan Sun	Miniature NMR systems for rock and outcrop analysis	Formation Evaluation Industry Consortium	$105K	2011-2014
PI: Nan Sun	Student design contest	Texas Instruments	$20K	2011-2018
PI: Nan Sun	Gift	Texas Instruments	$60K	2015
PI: Nan Sun	Gift	Texas Instruments	$60K	2014
PI: Nan Sun	Gift	Texas Instruments	$60K	2013
PI: Nan Sun	Gift	Silicon Labs	$30K	2019
PI: Nan Sun	Gift	Silicon Labs	$30K	2018
PI: Nan Sun	Gift	Silicon Labs	$30K	2017
PI: Nan Sun	Gift	Cirrus Logic	$20K	2019
PI: Nan Sun	Gift	Cirrus Logic	$20K	2018
PI: Nan Sun	Gift	Cirrus Logic	$20K	2017
PI: Nan Sun	Gift	Cirrus Logic	$20K	2016
PI: Nan Sun	Gift	Cirrus Logic	$20K	2015
PI: Nan Sun	Gift	Cirrus Logic	$20K	2014
PI: Nan Sun	Gift	Cirrus Logic	$20K	2013
PI: Nan Sun	Gift	Cirrus Logic	$20K	2012
PI: Nan Sun	Gift	MediaTek	$20K	2012
PI: Nan Sun	Gift	Intel	$30K	2012
PI: Nan Sun	Gift	Intel	$30K	2011

External In-Kind Donations (Total Market Value ≈ $1.3M)

	Free Integrated Circuit (IC) Fabrication	**Company**	**Donation in Value**	**Year**
Lead PI	25 mm^2 free IC fabrication in 180nm	TSMC	$30K	2019
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$180K	2019
Lead PI	25 mm^2 free IC fabrication in 180nm	TSMC	$30K	2018
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$180K	2018
Lead PI	Twice 25 mm^2 free IC fabrication in 180nm	TSMC	$60K	2017
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$180K	2017
Lead PI	4 mm^2 free IC fabrication in 130nm	MOSIS	$20K	2016
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$180K	2016
Lead PI	Twice 25 mm^2 free IC fabrication in 180nm	TSMC	$60K	2016
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	2015
Lead PI	Twice 9 mm^2 free IC fabrication in 40nm	TSMC	$90K	2015
Lead PI	25 mm^2 free IC fabrication in 180nm	TSMC	$30K	2015

Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	2015
Single PI	1 mm^2 free IC fabrication in 65nm	Texas Instruments	$10K	2014
Single PI	1 mm^2 free IC fabrication in 65nm	Samsung	$10K	2014
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	2014
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	2013
Lead PI	16 mm^2 free IC fabrication in 130nm	MOSIS	$75K	2012

Teaching Experiences

Course	Semester	Enrollment / Returned	Instructor / Course Rating
EE 438K: *Analog Electronics*	Spring 11	41 / 24	4.8 / 4.5
EE 338L: *Analog Integrated Circuit Design*	Spring 18	26 / 15	4.7 / 4.5
EE 338L/382M-14: *Analog Integrated Circuit Design*	Fall 12	55 / 37	4.5 / 4.3
	Fall 14	52 / 39	4.6 / 4.4
	Fall 15	53 / 33	4.3 / 4.0
EE 382M-14: *Analog Integrated Circuit Design*	Fall 16	26 / 16	4.6 / 4.7
	Fall 17	33 / 23	4.5 / 4.4
EE 382V: *Data Converters*	Spring 12	20 / 19	5.0 / 4.9
	Spring 13	15 / 14	4.9 / 4.8
	Spring 14	10 / 10	4.6 / 4.6
	Spring 15	10 / 9	4.8 / 4.3
	Spring 17	19 / 18	4.8 / 4.6

PhD Students Graduated

Student Name	Degree	Start Date	Graduation Date	Placement
Arindam Sanyal	PhD	09/2011	10/2015	Tenure-Track Assistant Professor at SUNY Buffalo
Wenjuan Guo	PhD	09/2011	02/2016	Intel
Long Chen	PhD	09/2011	05/2016	Broadcom
Kareem Ragab	PhD	09/2011	07/2016	Broadcom
Yeonam Yoon	PhD	09/2011	05/2017	Intel
Jeonggoo Song	PhD	09/2013	11/2017	Intel
Manzur Rahman	PhD	09/2012	11/2017	MediaTek
Raghunadan Raghunathan	PhD	11/2011	11/2017	Silicon Labs
Shaolan Li	PhD	09/2012	05/2018	Tenure-Track Assistant Professor at Georgia Institute of Technology
Xiyuan Tang	PhD	09/2012	07/2019	Post-doc at UT Austin
Linxiao Shen	PhD	09/2014	09/2019	Silicon Labs

Jointly Supervised PhD Students:

1. Zhelu Li, Joint PhD from Zhejiang University, China
2. Xin Xin, Joint PhD from Xidian University, China
3. Yi Shen, Joint PhD from Xidian University, China
4. Dengquan Li, Joint PhD from Xidian University, China
5. Jiaxin Liu, Joint PhD from University of Electronic Science and Technology, China
6. Haoyu Zhuang, Joint PhD from Xidian University, China
7. Yanlong Zhang, Joint PhD from Xidian University, China

8. Yi Zhong, Joint PhD from Beijing Institute of Technology, China

Master Students Graduated

Student Name	Degree	Start Date	Graduation Date	Placement
Marco Moreno	MS	09/2009	05/2012	Emerson
Harold Bautista	MS	09/2010	05/2012	AMD
Miguel Gandara	MS	09/2011	05/2012	PhD student at UT Austin
Alex Fontaine	MS	09/2011	05/2013	Applied Research Laboratories
Shitong Zhao	MS	09/2011	05/2013	Qualcomm
Xiankun Jin	MS	09/2011	05/2013	NXP
Olga Kardonik	MS	09/2011	05/2013	Intel
Kyoungtae Lee	MS	09/2012	05/2014	PhD student at UC Berkeley
Ji Ma	MS	09/2012	05/2014	Qualcomm
You Li	MS	09/2013	05/2015	Oracle
Anoosh Gnana	MS	09/2013	05/2015	McCombs School of Business
Phillippe Dollo	MS	09/2014	05/2016	Texas Instruments
Paridhi Gulati	MS	09/2014	05/2016	Analog Devices
Sowmya Katragadda	MS	09/2014	05/2016	Oracle
Xuming Zhao	MS	09/2015	05/2017	Intel
Vivek Varier	MS	09/2015	12/2017	Texas Instruments
Yunyi Wang	MS	09/2016	05/2018	Omnivision
Mantian Zhang	MS	07/2017	05/2019	MediaTek
Sudeep Mishra	MS	07/2017	05/2019	Silicon Labs

Current Graduate Students

Student Name	Degree	Status	Start Date	Completion
Miguel Gandara	Ph.D.	In Candidacy	Fall 2012	Spring 2020 (est.)
Sungjin Hong	Ph.D.	In Candidacy	Fall 2012	Spring 2020 (est.)
Abhishek Mukherjee	Ph.D.	Pre-candidacy	Fall 2014	Spring 2020 (est.)
Chen-Kai Hsu	Ph.D.	Pre-candidacy	Fall 2016	Spring 2020 (est.)
Wenda Zhao	Ph.D.	Pre-candidacy	Fall 2016	Spring 2021 (est.)
Xiangxing Yang	Ph.D.	Pre-candidacy	Fall 2017	Spring 2022 (est.)
Wei Shi	Ph.D.	Pre-candidacy	Fall 2017	Spring 2022 (est.)
Ahmet Dudak	Ph.D.	Pre-candidacy	Fall 2018	Spring 2023 (est.)
Arnab Dutta	Ph.D.	Pre-candidacy	Fall 2018	Spring 2023 (est.)

Visiting Graduate Students:

1. Zheng Yang, visiting PhD from University, China
2. Somayeh Abdollahvand, visiting PhD from University at Lisbon, Portugal
3. Begum Kasap, Joint master from ETH, Switzerland

Visiting Scholars:

1. Xili Han, Associate Professor from University of Electronic Science and Technology, China
2. Gang Jin, Associate Professor from Xidian University, China
3. Yanzhao Ma, Assistant Professor from Northwestern Polytechnical University, China
4. Ran Zheng, Assistant Professor from Northwestern Polytechnical University, China
5. Lei Zhang, Assistant Professor from Beijing Institute of Technology, China
6. Fanyang Li, Assistant Professor from Fuzhou University, China
7. Juha Kim, Design Engineer from Samsung, Korea
8. Ying Kong, Design Manager from Beijing Microelectronics Technology Institute, China
9. Lanchuan Zhou, Project lead from Institute of Astronomy, Chinese Academy of Sciences

Short Biography

Nan Sun is Temple Foundation Endowed Associate Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. He received the B.S. degree from Tsinghua University in 2006 and the Ph.D. degree from Harvard University in 2010. Dr. Sun received the NSF Career Award in 2013, and the Jack Kilby Research Award from UT Austin in both 2015 and 2016. He holds the AMD Endowed Development Chair from 2013 to 2017. He serves on the Technical Program Committee of the *IEEE Custom Integrated Circuits Conference* and the *IEEE Asian Solid-State Circuit Conference*. He is an Associate Editor of the *IEEE Transactions on Circuits and Systems – I: Regular Papers*, and a Guest Editor of the *IEEE Journal of Solid-State Circuits*. He also serves as IEEE Circuits-and-Systems Society Distinguished Lecturer from 2019 to 2020.