Mark McDermott, Ph.D., P.E.
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Profile: Extensive engineering management and design expertise in the implementation of integrated circuits and embedded systems. Strong working knowledge of nanometer VLSI design, embedded system design, structured product development processes, EDA tools and methodologies. Co-founded seven startup companies.

Strengths: Team building and leadership, communication skills, mentoring, infrastructure development, process analysis and development, business plan development, technical course development and teaching, product planning, hardware and software project/program management, system design/verification.

Education: University of Texas, Austin, Texas; Ph.D.
University of Texas, Austin, Texas; MSE
University of New Mexico, Albuquerque, N. M.; BSEE

Organizations: IEEE, ACM, TSPE

Related Work Experience:

1/01 – Present ***Professor of Practice & EIR, ECE Department, University of Texas, Austin, TX***

Currently doing research on cognitive sensor architectures for ultra-low-power biosensor applications. In addition, I teach undergraduate and graduate level classes in embedded system/circuit design including: Advanced VLSI Design, SOC Design, Embedded Systems Architecture.
Web site: http://www.ece.utexas.edu/~mcdermot/

4/10 – 8/14 ***Sr. Director, Apple Inc., Austin, Texas***

Responsible for the management of an SOC design team focused on the implementation of video and graphics IP.

8/09 – 4/10 ***GM & VP Engineering, Intrinsity Corp., Austin, Texas***

Brought in to the company to prepare it for an acquisition. Subsequently acquired by Apple, Inc.

3/06 – 8/09 ***CTO and Co-Founder, The Learning Labs, Inc., Austin, TX & Bangalore, India***

Startup company focused on developing hardware and software platforms for multidisciplinary system level design education. This was in support of my teaching work at the Univ. of Texas.

8/05 – 8/07 ***VP Engineering, Coherent Logix, Inc., Austin, Texas***

Startup company developing a multiprocessor DSP processor system for imaging and signal processing applications as part of a DARPA funded project.

6/04 – 8/05 ***CEO & Co-Founder, DynaFlow Computing, Inc., Austin, Texas***

Startup company whose mission was to commercialize the TRIPS (Tera-op Reliable Intelligently adaptive Processing System) that was developed at the University of Texas at Austin as part of a DARPA project.

12/03 – 5/04 ***VP Engineering & Co-Founder, Somerset Embedded Technologies, Inc., Austin, Texas***

Startup company that was formed to purchase the 4XX PowerPC assets from IBM. Obtained funding but did not win the bid.

4/03 – 12/03 ***VP Engineering & Co-Founder, VisionFlow, Inc., Austin, Texas***

Startup company focused on the development of hardware accelerators for video transcoding and transcription. Transferred to the technical advisory board after completing the startup phase.

9/98 – 3/03 ***Director & GM, Texas Development Center, Desktop Platform Group, Intel Corp, Austin, Texas***

Formed a 300+ person development center whose focus was on implementing the next generation design methodology for implementing high-performance microprocessors. This included recruiting the management, design, and EDA teams; setting up the operational infrastructure and the project management processes. The development team was responsible for the design of a next generation IA32 desktop processor and developing next generation EDA tools to support 90nm/65nm designs.

7/95 - 9/98 ***Director, Somerset Design Center, IBM/Motorola PPC Joint Development Group, Austin, Texas***

Responsible for the management of the joint IBM/Motorola PowerPC design center whose mission was the development of the 603, 604, 620, G3 and G4 microprocessors. Set up numerous operational and project management systems to improve design productivity and TTM. Revamped the product development process utilizing IPD (Integrated Product Development) methods.

8/91 - 7/95 ***Director, Austin Design Center, Cyrix Corp., Austin, Texas***

Setup the design center and managed the design of a low-power x86 microprocessor core, which became the 5X86 and the Media-GX processors. Responsibilities included: product definition, engineering management, design implementation of the PLL, clocking and testability circuits. Additional responsibilities included setting up the EDA design methodology, component modeling environment, and the DFT/DFM methodology.

6/90 - 8/91 ***Design Engineering Manager, Logical Silicon Solutions, Austin Texas***

Setup the design center and managed the design and layout engineering groups, EDA methodology and DFT. The center was responsible for the design of a BiCMOS secondary cache for the OKI Semiconductor TRON project.

10/88 - 6/90 ***Member of Technical Staff, MPU Design Group, Motorola, Inc. Austin, Texas***

Project leader on the 68050 & 88110 high performance RISC microprocessor. Responsibilities included management and design activities in the following areas: architecture, system and circuit design, EDA methodology, DFT, layout and CAD tools.

5/86 - 10/88 ***Member of Technical Staff, MCU Design Group, Motorola, Inc. Austin, Texas***

Circuit design and integration project leader on the MC68332 (GMPX) MCU. Responsibilities included system integration, logic/circuit design, process modeling and layout. Designed the Inter-module Bus, I/O circuits, PLL, global and local clocking circuits and power down detect circuits.

6/85 - 5/86 ***Principal Staff Engineer, Computer-X, Motorola New Enterprises, Austin, Texas***

Responsible for system and logic design, diagnostic software, manufacturing and parts procurement of VME processor boards for the CX factory automation computer system.

8/84 - 6/85 ***VP VLSI Design and Co-Founder, Accelerated Solutions Corp., Austin, Texas***

Co-founder of the company, whose primary product was a high performance class-solution EDA accelerator. Responsible for the design of the special purpose processors/accelerator ICs. Team was acquired by Motorola New Enterprises.

6/81 - 8/84 ***Senior Design Engineer, TEGAS Systems Inc., Austin, TX.***

Member of a team that designed and built a special purpose attached processor that performed digital logic simulation. This machine supported the TEGAS logic simulator. Responsibilities included the design implementation and testing of the Update Processor, Control Processor and the Descriptor Memory boards. Wrote all of the control and maintenance microcode for the two processors.

12/77 - 6/81 ***Design Engineer, CMOS Design Group, Motorola, Inc. Austin, Texas.***

IC design engineer with Custom/Special Function design group. Designs include MC146818 Real Time Clock chip, MC6175 Speech Synthesizer and the MC6185 SSU ROM. Designed numerous latch-up and process test vehicles. Published latch-up prevention guidelines and various other design guides.

5/75 - 12/77 ***IC Lab Manager, Bureau of Engineering Research, Univ. of New Mexico***

Responsible for the maintenance of the IC processing equipment in the research labs. Worked on numerous projects for Sandia Labs and Wright-Paterson AFB. This included the design of radiation-hardened CMOS test vehicles, various GaAs test structures and Ferro-Electric memory devices.

Patents: 71 disclosures, 19 issued:

5,926,053 Selectable clock generation mode
5,860,105 NDIRTY cache line look-ahead
5,815,693 Processor having a frequency modulated core clock based on the criticality of program activity
5,815,692 Distributed clock generator
5,740,410 Static clock generator
5,734,881 Detecting short branches in a prefetch buffer using target location information in a branch target cache
5,734,844 Bidirectional single-line handshake with both devices driving the line in the same state for hand-off
5,592,107 Configurable NAND/NOR element
5,568,067 Configurable XNOR/XOR element
5,448,744 Integrated circuit microprocessor with programmable chip select logic
5,402,458 Mechanism to accelerate counter testing without loss of fault coverage
5,361,392 Digital computing system with low power mode and special bus cycle therefor
5,233,314 Integrated charge-pump phase-locked loop circuit
5,157,781 Data processor test architecture
5,138,709 Spurious interrupt monitor
5,029,272 Input/output circuit with programmable input sensing time
4,959,561 MOS output buffer with reduced supply line disturbance
4,931,748 Integrated circuit with clock generator
4,366,560 Power down detector

Publications

A. Manickam, K. You, N. Wood, L. Pei, Y. Liu, R. Singh, N. Gamini, M. McDermott, D. Shahrjerdi, R. Kuimelis, A. Hassibi, "*A CMOS Electrochemical Biochip With 32x32 Three-Electrode Voltammetry Pixels*," in IEEE Journal of Solid-State Circuits (JSSC), Nov 2019

A. Hassibi, A. Manickam, R. Singh, S. Bolouki, R. Sinha, K. B. Jirage, M. McDermott, B. Hassibi, H. Vikalo, G. Mazarei, L. Pei, L. Bousse, M. Miller, M. Heshami, M. Savage, M. Taylor, N. Gamini, N. Wood, P. Mantina, P. Grogan, P. Kuimelis, P. Savalia, S. Conradson, Y. Li, R. Meyer, E. Ku, J. Ebert, B. Pinsky, G. Dolganov, T. Van, K. Johnson, P. Naraghi-Arani, R. Kuimelis & G. Schoolnik., "*Multiplexed identification, quantification and genotyping of infectious agents using a semiconductor biochip,*" Nature Biotechnology, Jul. 2018

A. Manickam, R. Singh, M. McDermott, N. Wood, S. Bolouki, P. Naraghi-Arami, R. G. Kuimelis, G. Schoolnik, A. Hassibi, "*A Fully Integrated CMOS Fluorescence Biochip for DNA and RNA Testing*," IEEE Journal of Solid-State Circuits, Vol. 52, No. 11, pp. 2857-2870, Nov. 2017

A. Hassibi, R. Singh, A. Manickam, R. Sinha, B. Kuimelis, S. Bolouki, P. Naraghi-Arani, K. Johnson, M. McDermott, N. Wood, P. Savalia, N. Gamini, , "*A Fully Integrated CMOS Fluorescence Biochip for Multiplex Polymerase Chain-Reaction (PCR) Processes*," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), Feb. 2017, San Francisco, CA

A. Manickam, A. Chevalier, M. McDermott, A.D. Ellington, A. Hassibi, "*A CMOS Electrochemical Impedance Spectroscopy (EIS) Biosensor Array*," Biomedical Circuits and Systems, IEEE Transactions on, pp. 379-390, Nov. 2010

M. McDermott, "*Queued-Stack Dataflow Processing Element for a Cognitive Sensor Platform*," International Journal of Reconfigurable and Embedded Systems (IJRES), Vol. 1, No 3, pp. 75-86, 2012

M. McDermott, "*Cognitive Sensor Platform*," International Journal of Electrical and Computer Engineering (IJECE), Vol. 4, No. 4, pp. 520-531, 2014

A. Manickam, A. Chevalier, M. McDermott, A.D. Ellington, A. Hassibi, "*A CMOS Electrochemical Impedance Spectroscopy Biosensor Array for Label-free Biomolecular Detection,*" Solid-State Circuits Conference Digest of Technical Papers (ISSCC), Feb. 2010, San Francisco, CA

J. Kulkarni, A. Sayal, P. Ajay, M. McDermott and S.V. Sreenivasan, "*A Design Methodology for High-Mix, Low-Volume Heterogeneously Integrated ASICs*," GOMAC Tech, 2019

R. Skruhak, M. McDermott, C. Wiseman, M. Taborn, J. Vaglica, E. Carter, "*Modular Design of a High Performance 32-bit Microcontroller*," Custom Integrated Circuits Conference, Proceedings of the IEEE," pp. 23.8/1 - 23.8/4, May 1989

M. Ravel and M. McDermott, "*An Electronic System Design Platform for SYSTEMatic Learning in ECE and ICT Curriculum*," 2007 Intl. Conf. on Microelectronic Systems Education (MSE 2007), pp. 145-146, 2007

M. Ravel, M. Chang, M. McDermott, M. Morrow, N. Teslic, M. Katona, J. Bapat, "*A Cross-Curriculum Open Design Platform Approach to Electronic and Computing Systems Education*," 2009 Intl. Conf. on Microelectronic Systems Education (MSE 2009), pp. 69 – 72, 2009

M. McDermott, J. Abraham, and M. Ravel, "*Balancing Virtual and Physical Prototyping Across a Multi-course VLSI/Embedded-Systems/SOC Design Curriculum*," In Proceedings of American Society for Engineering Education (ASEE) Annual Conference, pp. 14.270.1-14.270.8, 2009

S. Abdulla, H. Nam, M. McDermott, and J.A. Abraham, "*A High Throughput FFT Processor with no Multipliers*," Proc. IEEE Int. Conference Computer Design (ICCD), Lake Tahoe, CA, pp. 485-490, Oct. 2009

M. McDermott, "*Engineering Management Practices*," 2nd International Workshop on Engineering Management for Applied Technology (EMAT'01), 2001

W. Harwood, M. McDermott, "*Testability features of the MC68332 modular microcontroller*," Proceedings of International Test Conference *(1989*) pp. 615 – 623, 1989

J. Friesenhahn, L. John, and M. McDermott, "*Power Analysis of a Path-Based Perceptron Branch Predictor*," Austin Conference on Integrated Systems and Circuits (ACISC), May 2008.