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Research Interests:

- Machine learning hardware accelerators (Neuromorphic computing, compute-in-memory)
- Energy efficient integrated circuits (logic, memory, power management, hardware security)
- Applications of emerging technologies (STTRAM, RRAM, PCMs, crossbar arrays, 3DIC)

Education:

- **Purdue University,** West Lafayette, IN
  Ph.D. Electrical & Computer Engineering, 2009
  Dissertation: Low Voltage Robust Memory Circuit Design
  Advisor: Prof. Kaushik Roy
- **Indian Institute of Science (IISc)** Bangalore, India
  M. Tech. in Electronics Design and Technology, 2004
- **College of Engineering Pune (COEP),** University of Pune, India
  B. E. in Electronics and Telecommunication Engineering, 2002

Work Experience:

- Assistant Professor, The University of Texas at Austin, TX — August'17- Present
- Senior Staff Research Scientist, Intel Labs, Hillsboro, OR — May'09 – July'17
- Research Assistant, Purdue University, W. Lafayette, IN — Jul'05 – Apr'09
- Graduate Intern, Circuit Research Lab, Intel, Hillsboro, OR — May'08 – Aug'08
- Graduate Intern, Technology Manufacturing Group, Intel, Hillsboro, OR — May'07 – Aug'07
- Design Engineer, Cypress Semiconductor, Bangalore, India — Jul'04 – May'05
- Graduate Researcher, Indian Institute of Science, Bangalore, India — Jul'02 – May'05
- Graduate Intern, Texas Instruments, Bangalore, India — Jan'04 – May'04
- Undergraduate intern, Cirrus Logic, Pune, India — Jan'01 – Apr'02

Honors and Awards:

1. AMD endowed faculty chair in Computer Engineering, University of Texas at Austin (2017-present)
2. Industrial Distinguished Lecturer for IEEE Circuits and Systems (CAS) Society (2017)
3. SRC Mahboob Khan Outstanding Industry Liaison Award (2015)
4. IEEE Transactions on VLSI Systems Best Paper Award (2015)
5. IEEE Senior Member (2015)
6. Intel Corporation- 7 Divisional Recognition Awards (2009-2017)
7. Intel Corporation- 4 Patent Recognition Awards (2009-2017)
8. Outstanding Doctoral Dissertation Award by Purdue University's School of ECE (2010)
9. Intel Foundation Ph.D. Fellowship Award (2008-09)
10. Two SRC Inventor Recognition Awards (2008)
11. Best paper in session Award at SRC TECHCON (2008)
12. ISLPED Design Contest Award (2008)
13. Best M.Tech Student Award, CEDT Design Medal by IISc Bangalore (2004)
14. Pune University Junior and Senior Year Top-5 (Summa Cum Laude) Award (2001, 2002)
15. National Talent Search (NTS) Scholarship by the Government of India (1996-2002)

Professional Activities:

1. Chair, IEEE CASS/SSCS Central Texas Chapter (2020-present)
2. Associate Editor, IEEE Solid State Circuits Letters, (2018-present)
3. Associate Editor, IEEE Transactions on VLSI systems, (2015-present)
4. Guest Editor, IEEE Micro, Special Issue on Circuits 2020
5. Member of IEEE CAS Society – VLSI systems and applications technical committee (2015-present)
6. Senior Member – IEEE, Solid State Circuits, Circuits and Systems, and Electron Device Society
7. IEEE Conference Organization –
    - General Co-chair, 2018, International Symposium on Low Power Electronics Design (ISLPED)
    - Technical program co-chair, 2017 International Symposium on Low Power Electronics Design
8. IEEE Conference Technical Program Committee Member –
    - AI Circuits and Systems Conference (AICAS, 2020)
    - Custom Integrated Circuits Conference (CICC, 2019-present)
    - International Conference on Computer-Aided Design (ICCAD, 2018-present)
    - Design Automation Conference (DAC, 2018-2019)
    - International Conference on VLSI Design (VLSID, 2019)
    - Dallas Circuits and Systems Conference (DCAS, 2018)
    - International Symposium on Quality Electronics Design (ISQED, 2019)
    - Asian Solid State Circuits Conference (A-SSCC, 2014-2017)
    - International Conference on Computer Design (ICCD, 2017)
    - International Symposium on Circuits and Systems (ISCAS, 2016)
    - International Symposium on Low Power Electronics Design (ISLPED, 2013-2016)

- Asian Symposium on Quality Electronics Design (ASQED, 2010-13)

9. IEEE Conference Service:
   - Best paper award committee member, VLSI Design Conference, India 2018
10. Member – Association of Computing machinery (ACM), Special Interest Group on Design Automation (SIGDA)
11. Industrial Liaison/Associate (2009-2017)–
    - Stanford University - SystemX Alliance, Non-volatile Memory Technology Research Initiative (NMTRI)
    - Semiconductor Research Corporation (SRC) – Integrated Circuits and Systems Track
    - NSF program on Visual Cortex on Silicon (Penn State, MIT, USC, UCSD, UCLA, Stanford, Notre Dame, Univ. of Pittsburgh, York College)
    - STARnet Research - Systems On Nanoscale Information fabriCs Center (SONIC); Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN); Center for Low Energy Systems Technology (LEAST)
    - Technical Champion, Intel Academic Research Office program on "Post-CMOS Circuits and Architectures"
12. Reviewer:
    - IEEE Micro
    - IEEE Journal of Solid State Circuits
    - IEEE Transactions on Circuits and Systems – I and II
    - IEEE Transactions on VLSI Systems
    - VLSI Circuit Symposium
    - IEEE Transactions on Computers
    - IEEE Transactions on Electron Devices
    - IEEE Electron Device Letters
    - IEEE Journal on Emerging and Selected Topics in Circuits and Systems
    - ACM Journal on Emerging Technologies in Computing

Current students:

1. Sai Subrahma Nibhanupudi, Ph.D. student, (Fall'2017-)
2. Aseem Sayal, Ph.D. student (Co-advised by Prof. S.V. Sreenivasan), (Spring'2018-)
3. Rahul Mathur, Ph.D. student, (Fall'2018-)
4. Jacob Rohan, Ph.D. student, (Fall'2018-)
5. Meizhi Wang, Ph.D. student, (Fall'2018-)
6. Shanshan Xie, Ph.D. student, (Spring'2019-)
7. Rishabh Sehgal, Ph.D. student, (Fall'2019-)
8. Stafford Hutchins, Ph.D. student, (Fall'2019-)
9. Siddhartha Raman Sundara Raman, M.S. student, (Fall'2019-)
10. Can Ni, M.S. student, (Fall'2019-)

Graduated students:

1. Shirin Fatima, M.S. Spring 2019, Thesis Title: “All-Digital Time-Domain CNN Engine for Energy Efficient Edge Computing”
2. Naman Maheshwari, M.S. Spring 2019, Thesis Title: “Estimating the Minimum Bit-Width Precision for Stable Deep Neural Networks Utilizing Numerical Linear Algebra”
3. Wei Li, M.S. Spring 2019, Thesis Title: “An Energy Efficient Compute-in-Memory SRAM for Low Power CNN based Machine Learning Application”

Ph.D. Committee Member – UT Austin:

1. Paras Ajay, “Nano-precise Alignment for Advanced Lithography and Pick-and-Place Assembly”, Ph.D. Student, Electrical and Computer Engineering Department, Graduation: Fall 2019
2. Heechai Kang, Thesis Title: “Broadband Receivers Employing Pulse-Width-Modulation”, Ph.D. Student, Electrical and Computer Engineering Department, Graduation: Fall 2019
3. Crystal Baker, Thesis Title: “Radiation damage to image sensors”, Ph.D. Student, Nuclear and Radiation Engineering program, Mechanical Engineering Department, Expected Graduation: 2020
4. Xin Zhao, Thesis Title, “Design of A Plug-and-Play Single Stage AC/AC Medium Voltage Modular Solid-State Transformer based on LLC Resonant Converter and an Input-Series-Output-Parallel Architecture” Electrical and Computer Engineering Department, Expected Graduation: 2020

Ph.D. Committee Member – Outside of UT Austin:

5. Ankit Sharma, Thesis Title: “Sub-10nm Tunnel FETs” Ph.D. ECE, Purdue University, March 2018
6. Kenneth Ramclam, Thesis Title: “Low-Power and Robust Level-Shifter with Contention Mitigation for Memory and Standalone Applications” M.S. CSE, University of South Florida, March 2015

K-12 student mentoring:

1. Parth Shroff, LASA High School, Austin (Fall’2018-2019)

Teaching:

1. EE 316, Digital Logic Design, Fall 2019 (Under Graduate)
2. EE 382.8M, VLSI-II, Spring 2019 (Graduate), Instructor rating: 4.8/5.0, Course rating: 4.6/5.0
3. EE 382.8M, VLSI-II, Spring 2018 (Graduate), Instructor rating: 4.3/5.0, Course rating: 4.0/5.0
4. EE 464, Senior Design project, Fall 2017-Fall 2018, Spring 2019, Fall 2019

University Service:

1. Selection Panellist for UT competition sponsored by Office of Vice President for Research, 2019
2. Junior faculty hiring committee, ECE Department, UT Austin, 2019-2020
3. Colloquium Series committee, ECE Department, UT Austin, 2019-2020
4. Junior faculty hiring committee, ECE Department, UT Austin, 2018-2019
5. Integrated Circuits and Systems graduate admissions committee, 2017-present
6. Participated in junior faculty selection process, UT Austin, 2017-2018

Student Outreach:

1. Career panel presentation on faculty job preparation, Graduate Engineering Council (GEC), Cockrell School of Engineering, Fall 2019
2. Co-ordinator for the Integrated circuits area for incoming graduate student site visit, Spring 2019
3. Student technical area advising, HKN Technical Area night, Spring 2018

Invited Seminars, Keynotes, Short Course, and Tutorials:

T1. "All-Digital Time-Domain CNN Engine Using Bi-Directional Memory Delay Lines for Energy-Efficient Edge Computing" Silicon Labs, Austin, TX, November 2019

T2. **Invited Talk**, "High Density Non-Volatile SRAM using RRAM and Selector as Technology Assist", IEEE Non-Volatile Memory Technology Symposium (NVMTS), Durham, NC, October 2019

T3. "All-Digital Time-Domain CNN Engine Using Bi-Directional Memory Delay Lines for Energy-Efficient Edge Computing" Qualcomm, Raleigh, NC, October 2019

T4. **Keynote Talk** "Energy Efficient Embedded Memories in Advanced CMOS: Trends and Prospects", VLSI Design and Test Conference, Indian Institute of Technology (IIT), Indore, India, July 2019

T5. **Invited Talk** "Embedded Memories in Advanced CMOS: Trends and Opportunities in ML/AI Accelerators", Indian Institute of Technology (IIT) Bombay, India, July 2019

T6. "Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators" Samsung R&D Institute, Bangalore, India, July 2019

T7. "Embedded memories in advanced CMOS: Trends and Prospects" Qualcomm Bangalore, India, July 2019

T8. "Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators" ARM, Bangalore, India, July 2019

T9. "Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators" **Invited Talk**, IEEE Chapter University Visvesvaraya College of Engineering (UVCE), Bangalore, India, July 2019

T10. "Threshold switching selector devices for energy efficient integrated circuits", **Invited Talk**, IEEE EDS/SSCS Bangalore Chapter, Indian Institute of Science (IISc), Bangalore, India, July 2019

T11. "Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators", **Keynote Talk,** IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), Bangalore, India, July 2019

T12. "Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators" **Invited Talk**, College of Engineering Pune (COEP), India, July 2019

T13. "Circuit Technologies for efficient in-memory computing" **Invited short course** at International Memory Workshop (IMW), Monterey, CA, May 2019

T14. "Phase transition material assisted energy efficient CMOS design" Workshop on microelectronics and Electron Devices (WMED), IEEE Boise Chapter, **Invited Talk**, Boise, ID, April 2019

T15. "Phase transition material assisted energy efficient CMOS design" Silicon Labs, Austin, TX, August 2018

T16. "Phase transition material assisted energy efficient CMOS design" Intel, Hillsboro, OR, July 2018

T17. “Energy Efficient memories design for the compute continuum and beyond” Cirrus Logic, Austin, TX June 2018

T18. “Phase transition material assisted energy efficient SRAM design” Texas Instruments, Dallas, TX, May 2018

T19. “Energy Efficient memories design for the compute continuum and beyond” AMD, Austin, TX April 2018

T20. “Energy Efficient memories design for the compute continuum and beyond” ARM, Austin, TX February 2018

T21. “Energy Efficient memories for ultra-low power IoT applications”, Silicon Labs, Austin, TX, November 2017

T22. “Energy Efficient memory design for the compute continuum and beyond” UT Austin ECE Colloquium, November 2017

T23. “Energy Efficient memory design for the compute continuum and beyond” IEEE Santa Clara Valley Circuits and Systems Society, May 2017

T24. “Energy Efficient Memory Circuits: From IoT to Exascale Systems and Beyond”, University of Southern California, April 2016

T25. “Embedded Memory Design for Future Technologies: Challenges, Solutions and Applications” Tutorial at Design, Automation and Test Conference (DATE), March 2015

T26. “Process Adaptive Sub-Threshold Design”, Defense Advanced Research Projects Agency (DARPA), Washington D.C., October 2008

T27. “Write Current Reduction in MRAMs using Tiny Spiral Inductors’, 2008 International Solid State Circuits Conference (ISSCC), Student Forum, February 2008

T28. “Process Variation Tolerant SRAM Design for Ultra-Low Voltage Applications”, Indian Institute of Science, Bangalore, January 2008

T29. “Low-Power Robust CMOS Circuits for Scaled Technologies”, SRC Integrated Circuits and Systems Sciences, University of Massachusetts, Amherst, October 2007

Panels:

PN1. **“**Security and Trust as New Dimensions in Analog / RF Design Space Exploration**”** TxACE STARS: TxACE Workshop on Secure and Trusted Analog/RF Systems, UT Dallas, May 2018

PN2. “Magnetics, Logic and Memories Proposal Panel”, NSF, Washington D.C., March 2018

Patents:

P1. S.V. Sreenivasan, A. Mallavarapu, **J. P. Kulkarni**, S. Banerjee and M. Watts, “Three-dimensional SRAM architectures using catalyst influenced chemical etching” filed USPTO

P2. S.V. Sreenivasan, P. Ajay, A. Sayal, M. McDermott, **J. Kulkarni, “**Novel nanofabrication and design techniques for 3D ICs, and Configurable ASICs” filed USPTO

P3. S.V. Sreenivasan, P. Ajay, A. Sayal, A. Ovadia, M. McDermott, **J. Kulkarni**, and S. Shrawan, “Nanoscale aligned 3D stacked integrated circuit” filed USPTO 17/62609891, PCT/ WO2019126769A1

P4. A. Bonetti**, J. P. Kulkarni**, C. Tokunaga, M. Cho, P. Meinerzhagen, and M. Khellah, “Voltage level shifter monitor with tunable voltage level shifter replica circuit” filed USPTO 15394296

P5. **J. P. Kulkarni**, V. De and M. Khellah, “Aging aware dynamic keeper apparatus and associated method”, filed USPTO 15/604519

P6. **J. P. Kulkarni**, and M. Khellah, “Low swing bitline for sensing arrays” filed USPTO, 15/485,059

P7. M. Cho, **J. P. Kulkarni**, C. Tokunaga, M. Khellah, and J. Tschanz “Adaptive voltage system for aging guard-band reduction” filed USPTO 15/477913

P8. M. Cho, **J. P. Kulkarni**, C. Tokunaga, M. Khellah, and J. Tschanz “Retention minimum voltage determination techniques” USPTO 15373048

P9. A. Thaploo, **J. Kulkarni**, B. Borole, A. Appu, A. Koker, K. Sinha, W. Fu, “System, apparatus and method for reducing voltage swing on an interconnect” filed, USPTO 15/488,673

P10. **J. P. Kulkarni**, Y. Shim, and P. Meinerzhagen, “Apparatus and method for reducing di/dt” filed USPTO 15/163,494

P11. **J. P. Kulkarni**, Y. Shim, P. Meinerzhagen, M. Khellah “Bi-directional, multi-mode charge pump” filed USPTO 15/81445

P12. **J. P. Kulkarni**, I. Rajwani, and E. Donkoh, “Reduced swing bitline apparatus and method” US Patent 9,947,388

P13. F. Sheikh, A. Sharma, and **J. P. Kulkarni**, “Fast Fourier transform architecture” filed PCT/US2015/66963

P14. H. Bonakdar, **J.P. Kulkarni**, “Register files including distributed capacitor circuit blocks”, US Patent 9767858

P15. Y. Shim, **J. P. Kulkarni**, P. Meinerzhagen, and M. Khellah, “di/dt reduction technique during primary power gate wake-up”, US Patent 9755631

P16. **J. P. Kulkarni**, “Memory device including encoded data-line multiplexer” US Patent 9905278

P17. **J. P. Kulkarni**, P. Kolar, A. Sharma, S. Chatterjee, K. Subramanian, F. Sheikh, W. H. Ma, “Capacitive wordline boosting” filed USPTO 14/752464

P18. **J. P. Kulkarni**, A. Ravi, D. Somasekhar, G. Balamurugan, S. Shekhar, T. Musah, and T.-C. Hsueh “Digitally trimmable integrated resistors using resistive memory devices” US Patent 9589615

P19. A. Trivedi, **J. P. Kulkarni**, D. Somasekhar, M. Khellah, C. Tokunaga, J. Tschanz, “Current Steering Level Shifter” US Patent 9621163

P20. A. Trivedi, **J. P. Kulkarni**, C. Tokunaga, M. Khellah, J. Tschanz, “Voltage level shifter circuit” US Patent 9385722

P21. **J. P. Kulkarni**, A. Thaploo, I. Rajwani, K. Koo, E. Karl, M. Khellah, “Assist circuit for memory” US Patent 9355694

P22. **J. P. Kulkarni**, P. Meinerzhagen, D. Somasekhar, J. Tschanz, and V. De “Apparatus for charge recovery during low power mode” US Patent 9948179

P23. **J. P. Kulkarni**, B. Geuskens, J. Tschanz, V. De and M. Khellah “Methods and systems to selectively boost an operating voltage of, and controls to an 8T bit-cell array and/or other logic blocks” US Patent 9,633,716

P24. **J. P. Kulkarni**, K. Bowman, J. Tschanz and V. De “Resilient register file circuit for dynamic variation tolerance and method of operating the same” US Patent 9329918

P25. J. Nasrullah, K. Kwan, **J. P. Kulkarni** and M. Khellah "Method and systems for energy efficiency and energy efficiency and energy conservation including entry and exit latency reduction for low power states", US Patent 9665144

P26. I. Rajwani, S. Damaraju, N. Cooray, M. Khellah and **J. P. Kulkarni** "Memory array with extended write operation" USPTO/12642444

P27. P. Meinerzhagen, **J. P. Kulkarni**, M. Khellah, C. Dray, D. Somasekhar, J. Tschanz and V. De "Apparatus for dual purpose charge pump" US Patent 9,230,636

P28. **J. P. Kulkarni**, M. Khellah, J. Tschanz, B. Geuskens, and V. De "Apparatus for reducing write minimum supply voltage for memory" US patent 9,153,304

P29. A. Raychowdhury, **J. P. Kulkarni**, and J. Tschanz "Multi-supply sequential logic unit" US patent 8,901,819

P30. **J. P. Kulkarni**, D. Somasekhar "Low voltage swing repeater" US patent 8,847,633

P31. C. Wilkerson, A. Alameldeen, and **J. P. Kulkarni**, "Adaptive self-repairing cache" US patent 8,719,502

P32. **J. P. Kulkarni**, D. Somasekhar, J. Tschanz and V. De "Circuits and methods for memory" US patent 8488390

P33. **J. P. Kulkarni**, M. Khellah, B. Geuskens, A. Raychowdhury, T. Karnik and V. De "Memory write operation methods and circuits" US patent 8467263

P34. **J. P. Kulkarni** and K. Roy "Static random access memory cell and devices using the same", US patent 7952912

P35. **J. P. Kulkarni** and K. Roy "Memory cell with built-in process variation tolerance" US patent 7672152

Publications:

h-index = 22, total citations = 2950 (Google Scholar, 2nd December 2019)

Book / Book Chapters:

B1. **J. P. Kulkarni**, J. Tschanz and V. De, "Energy-Efficient Volatile Memory Circuits" in Enabling the Internet of Things - from Circuits to Networks, Editor: Prof. Massimo Alioto, Springer, New York, ISBN: 978-3-319-51480-2

B2. **J. P. Kulkarni** and K. Roy, "Technology/Circuit Co-design for III-V FETs" pp. 423-442, in Fundamentals of III-V Semiconductor MOSFETs, Springer, New-York 2010, ISBN: 978-1-4419-1546-7

Journal Papers:

J1. A. Sayal, P. Ajay, M. McDermott, S.V. Sreenivasan and **J. P. Kulkarni,** "M2A2: Microscale Modular Assembled ASICs for High-Mix, Low-Volume, Heterogeneously Integrated Designs" IEEE Transactions on Computer Aided Design (**TCAD**) (revision under review)

J2. A. Sayal, S. Fatima, S. S. Teja Nibhanupudi, and **J. P. Kulkarni**, "A 12.08 TOPS/W All-Digital Time-Domain CNN engine using Bi-directional Memory Delay Lines for Energy Efficient Edge Computing", IEEE Journal of Solid State Circuits (**JSSC**), pp. 60-75, Vol. 55, No. 1, January 2020, Invited paper for Special issue on ISSCC 2019

J3. P. Meinerzhagen, C. Tokunaga, A. Malavasi, V. Vaidya, A. Mendon, D. Mathaikutty, **J. Kulkarni**, C. Augustine, M. Cho, S. Kim, G. Matthew, R. Jain, J. Ryan, C.-C. Peng, S. Paul, S. Vangal, B. P.

Esparza, L. Cuellar, M. Woodman, B. Iyer, S. Maiyuran, G. Chinya, X. Zou, Y. Liao, K. Ravichandran, H. Wong, M. Khellah, J. Tschanz, and V. De, "An Energy-Efficient Graphics Processor in 14nm Tri-Gate CMOS Featuring Integrated Voltage Regulators for Fine-Grain DVFS, Retentive Sleep, and V_{MIN} Optimization" invited to IEEE Journal of Solid State Circuits (**JSSC**) Special issue on ISSCC 2018, pp. 144-157, Vol. 54, No. 1, January 2019

J4. S. Motaman, S. Ghosh, and **J. Kulkarni, "**VFAB: A Novel 2-Stage STTRAM Sensing Using Voltage Feedback and Boosting" IEEE Transactions on Circuits and Systems-I (**TCAS-I**), pp. 1919-1928, Vol. 65, issue-6, June 2018

J5. S. Motaman, S. Ghosh, and **J. Kulkarni**; "Impact of Process Variation on Self-Reference Sensing Scheme and Adaptive Current Modulation for Robust STTRAM Sensing" ACM Journal on Emerging Technologies in Computing Systems (**JETC**), pp. 1-17, Vol. 14, issue-1, October 2017

J6. **J. P. Kulkarni**, J. Keane, K.-H Koo, S. Nalam, Z. Guo, E. Karl, and K. Zhang, "5.6Mb/mm^2 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology" IEEE Journal of Solid State Circuits (**JSSC**) (special issue on ISSCC 2016), pp. 229-239, Vol. 52, No. 1, January 2017

J7. M. Cho, S. Kim, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, V. De, "Post-Silicon Voltage Guard-Band Reduction in a 22nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating" accepted to IEEE Journal of Solid State Circuits (**JSSC**), (special issue on ISSCC 2016), pp. 50 – 63, Vol. 52, No. 1, January 2017

J8. S. Srinivasa, A. Aziz, N. Shukla, X. Li, J. Sampson, S. Datta, J. P. Kulkarni, V. Narayanan, and S. Gupta, "Correlated Material Enhanced SRAMs with Robust Low Power Operation" IEEE Transactions on Electron Devices (**TED**), pp. 4744- 4752 Vol. 63, No. 12, December 2016

J9. A. Sharma, A. A. Goud, J. P. Kulkarni, and K. Roy, "Source-underlapped GaSb-InAs TFETs with applications to Gain Cell Embedded DRAMs" IEEE Transactions on Electron Devices (**TED**), pp. 2563-2569, Vol 63, No. 6, June 2016

J10. **J. P. Kulkarni**, C. Tokunaga, P. Aseron, T. Nguyen Jr, C. Augustine, J. Tschanz, V. De, "A 409 GOPS/W Adaptive & Resilient Domino Register File in 22nm Tri-Gate CMOS Featuring In-Situ Timing Margin & Error Detection for Tolerance to Within-Die Variation, Voltage Droop, Temperature & Aging, IEEE Journal of Solid State Circuits (**JSSC**), pp. 117-129, Vol. 51, No. 1, January 2016 Special issue on ISSCC 2015

J11. S. Kim, Y.-C. Shih, K. Mazumdar, R. Jain, J. Ryan, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, and V. De, "Enabling Wide Autonomous DVFS in a 22nm Graphics Execution Core Using a Digitally Controlled Fully Integrated Voltage Regulator" IEEE Journal of Solid State Circuits (**JSSC**), pp. 18-30, Vol. 51, No. 1, January 2016 Special issue on ISSCC 2015

J12. R. Jain, B. Geuskens, M. Khellah, S. Kim, **J. Kulkarni**, J. Tschanz and V. De, "A 0.45-1V Fully Reconfigurable Switched Capacitor step down DC-DC converter with High Density MIM Capacitor in 22nm Tri-gate CMOS" IEEE Journal of Solid State Circuits (**JSSC**), pp. 1-11, vol. 49, No. 4, April 2014

J13. R. Pandey, V. Saripalli, **J. P. Kulkarni**, S. Datta, "Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability", IEEE Electron Device Letters (**EDL**), pp. 393-395, Vol 35, No. 3, March 2014

J14. S. Gupta, **J.P. Kulkarni**, and K. Roy, "Tri-Mode Independent Gate FinFET based SRAM with Pass Gate Feedback: Technology-Circuit Co-design for Enhanced Cell Stability", IEEE Transactions on Electron Devices (**TED**), pp. 3696-3704, vol. 60, No. 11, November 2013

J15. A. R. Alameldeen, N.S. Kim, S. M. Khan, H. R. Ghasemi, C. Wilkerson, **J. Kulkarni**, D. A. Jimenez, "Improving memory reliability power and performance using mixed cell designs" Intel Technology Journal (**ITJ**), pp. 36-53, vol. 17, issue 1, 2013

J16. S. Gupta, **J.P. Kulkarni**, S. Datta and K. Roy, “Heterojunction Intra-band Tunnel (HIBT) FETs for Low Voltage SRAMs”, IEEE Transactions on Electron Devices (**TED**), pp. 3533-3542, vol. 59, No. 12, December 2012

J17. **J. P. Kulkarni** and K. Roy, "Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design” IEEE Transactions on VLSI systems (**TVLSI**), pp. 319-332, vol. 20, No. 2, February 2012 (**2015 IEEE TVLSI best paper award, Top-25 most downloaded TVLSI manuscript for the year 2012**)

J18. **J. P. Kulkarni**, A. Goel, P. Ndai and K. Roy, "Read-Disturb-Free, Differential Sensing 1R/1W Port 8T Bitcell Array” IEEE Transactions on VLSI systems (**TVLSI**), pp. 1727-1730, Vol. 19, Issue: 9, September 2011

J19. M. Meterelliyoz, P. Song, F. Stellari, **J. P. Kulkarni** and K. Roy, “Characterization of Random Process Variations using Ultra Low Power High Sensitivity, Bias Free Sub-threshold Process Sensor” IEEE Transactions on Circuits and Systems-I (**TCAS-I**), pp. 1838-1847, Vol. 57, Issue:8, August 2010

J20. **J. P. Kulkarni**, C. Augustine, B. Jung and K. Roy, "Nano-Spiral Inductors for Low Power Digital Spintronic Circuits” IEEE Transactions on Magnetics (**TMAG**), pp. 1898-1901, vol. 46, No. 6, June 2010

J21. M. Meterelliyoz, **J. P. Kulkarni** and K. Roy, “Analysis of SRAM and eDRAM Cache Memories under Spatial Temperature Variations” IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (**TCAD**), pp. 2-13, Vol. 29, Issue 1, January 2010

J22. **J. P. Kulkarni** and K. Roy, “Technology Circuit Co-design for Ultra-Fast InSb Quantum Well Transistors”, IEEE Transactions on Electron Devices (**TED**), pp. 2537-2545, Vol. 55, October 2008

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C1. R. Mathur, X. Xu, A. Chao, P. Chandupatla, S. Hung, N. Tadepalli, S. Sinha, and **J. Kulkarni**, “Thermal Analysis of a 3D Stacked High-Performance Commercial Microprocessor using Face-to-Face Wafer Bonding Technology”, 70th Electronic Components and Technology Conference (**ECTC**), May 2020 (accepted)

C2. **J. P. Kulkarni,** A. Sayal, S. S. Teja Nibhanupudi, and S. Fatima, “All-Digital Time-Domain CNN engine using Bi-directional Memory Delay Lines” Government Microelectronic Conference (**GOMACTech**), March 2020 (accepted)

C3. **J. P. Kulkarni,** and S. S. Teja Nibhanupudi, “Non-volatile SRAM leveraging novel materials” Government Microelectronic Conference (**GOMACTech**), March 2020 (accepted)

C4. J. N. Rohan, P. Zhuang, S. S. Teja Nibhanupudi, S. K. Banerjee, and **J. P. Kulkarni, “**Machine Learning Assisted Compact Modeling of Cycle-to-cycle Variations in 2-D h-BN based RRAM devices” Government Microelectronic Conference (**GOMACTech**), March 2020 (accepted)

C5. D. Prasad, S. S. Teja Nibhanupudi, S. Das, O. Zografos, B. Chehab, S. Sarkar, R. Baert, A. Robinson, A. Spessot, P. Debacker, D. Verkest, **J. Kulkarni**, B. Cline and S. Sinha, “Buried Power

Rails and Back-side Power Grids: Arm® CPU Power Delivery Network Design Beyond 5nm", IEEE International Electron Device Meeting (**IEDM**), pp. 446-449, December 2019

C6. J. N. Rohan, P. Zhuang, S. S. Teja Nibhanupudi, S. K. Banerjee, and **J. P. Kulkarni**, "Neural network assisted compact model for accurate characterization of Cycle-to-cycle variations in 2-D h-BN based RRAM devices" Device Research Conference (**DRC**), June 2019

C7. S. S. Teja Nibhanupudi, and **J.P. Kulkarni,** "High density NV-SRAM using memristor and selector as technology assist" IEEE International Symposium on VLSI Technology, Systems and Applications (**VLSI-TSA**), April 2019 (**Best Student Paper Nomination**)

C8. **J. P. Kulkarni**, and S. Teja, **"**Radiation Hardened Memory and Logic Design using Phase Transition Material' Government Microelectronic Conference (**GOMACTech**), March 2019

C9. **J. P. Kulkarni**, A. Sayal, P. Ajay, M. McDermott, and S. V. Sreenivasan; "A Design Methodology for High-Mix, Low-Volume, Heterogeneously Integrated ASICs" Government Microelectronic Conference (**GOMACTech**), March 2019

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C11. S. Teja, A. Rai, A. Roy, S. Banerjee, and **J.P. Kulkarni,** "Memory and Logic soft error improvement using phase transition material assisted transistors" IEEE International Conference on Emerging Electronics (**ICEE**), December 2018

C12. S. Teja, and **J.P. Kulkarni,** "Soft-FET: Phase transition material assisted Soft switching Field Effect Transistor for supply voltage droop mitigation" Design Automation Conference (**DAC**), June 2018

C13. S. Teja, and **J.P. Kulkarni,** "Phase Transition Material assisted circuits for improved soft error tolerance" Silicon Errors in Logic – System Effects Workshop (**SELSE**), March 2018

C14. P. Meinerzhagen, C. Tokunaga, A. Malavasi, V. Vaidya, A. Mendon, D. Mathaikutty, J. Kulkarni, C. Augustine, M. Cho, S. Kim, G. Matthew, R. Jain, J. Ryan, C.-C. Peng, S. Paul, S. Vangal, B. P. Esparza, L. Cuellar, M. Woodman, B. Iyer, S. Maiyuran, G. Chinya, X. Zou, Y. Liao, K. Ravichandran, H. Wong, M. Khellah, J. Tschanz, and V. De, "An Energy-Efficient Graphics Processor Featuring Fine-Grain DVFS with Integrated Voltage Regulators, Execution-Unit Turbo, and Retentive Sleep in 14nm Tri-Gate CMOS" International Solid State Circuits Conference (**ISSCC**), pp. 38-39, February 2018

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C17. J. Keane, **J. Kulkarni**, K.-H Koo, S. Nalam, Z. Guo, E. Karl, and K. Zhang, "5.6Mb/mm^2 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology" International Solid State Circuits Conference (**ISSCC**), pp. 308-309, Feb. 2016

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C22. C. Tokunaga, J. Ryan, C. Augustine, **J. Kulkarni**, Y. Shih, S. Kim, R. Jain, K. Bowman, A. Raychowdhury, M. Khellah, J. Tschanz, V. De, "A 22nm Graphics Execution Core with Wide Voltage Range and 40% Higher Peak GFLOPS/W via Adaptive Clocking, Selective Boosting, and State-Retentive Sleep" International Solid State Circuits Conference (**ISSCC**), pp. 108-109, February 2014

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C25. S. M. Khan, A. R. Alameldeen, C. Wilkerson, **J. Kulkarni**, D. A. Jimenez, "Improving Multi-Core Performance Using Mixed-Cell Cache Architecture", International Symposium on High Performance Computer Architecture (**HPCA**), pp. 229-230, February 2013

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C30. B. Geuskens, M. Khellah, **J. Kulkarni**, T. Karnik and V. De "Opportunities for PMOS Read and Write Ports in Low Voltage Dual-Port 8T Bit-Cell Arrays" Custom Integrated Circuits Conference (**CICC**), pp. 1-4, September 2010

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C38. K. Roy, **J.P. Kulkarni** and M.E. Hwang, "Process Adaptive Digital Sub-threshold Logic and Memory" 16th International Conference on Very Large Scale Integration (**VLSI-SOC**), pp. 42-45, October 2008 (Invited paper)

C39. **J. P. Kulkarni**, K. Kim, S. Park and K. Roy, "Process Variation Tolerant SRAM Array for Ultra Low Voltage Applications" Design Automation Conference (**DAC**), pp. 108-113, June 2008

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C42. M. Meterolliyez, **J. P. Kulkarni** and K. Roy, "Thermal Analysis of 8-T SRAM for Nano-scaled Technologies" International Symposium on Low Power Electronics Design, (**ISLPED**), pp. 123-128, August 2008

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C46. **J. P. Kulkarni** and N. Bhat, "Effect of Poly-Si Gate Depletion on Tuning Range of MOS Varactors" Device Research Conference (**DRC**), pp. 81-82, June 2006

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C48. A. Pugalia, **J. P. Kulkarni**, N. Bhargava and N. Bhat “Single pocket Halo Sensitivity in 100nm Analog Transistor Design” Intl. Workshop on Physics of Semiconductor Devices (**IWPSD**), pp. 611-613, December 2003

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C50. S. S. Teja Nibhanupudi, and **J.P. Kulkarni, “**High Density NV-SRAM using Memristor and Selector as Technology Assist” **ARM Research Summit**, September 2019

C51. S. S. Teja Nibhanupudi, and **J.P. Kulkarni, “**High Density NV-SRAM using Memristor and Selector as Technology Assist” **SRC TECHCON**, September 2019

C52. A. Sayal and J. P. Kulkarni, “All-Digital Time-Domain CNN Engine for Energy Efficient Edge Computing,” in ACM SIGDA and IEEE CEDA Ph.D. Forum at IEEE Design Automation Conference (**DAC**), June 2019

C53. **J. P. Kulkarni**, C. Augustine, B. Jung and K. Roy, "Nano-Spiral Inductors for Low Power Digital Spintronic Circuits” International Magnetics Conference (**INTERMAG**), January 2010

C54. **J. P. Kulkarni** and K. Roy, “Process Variation Tolerant SRAM Design for Ultra Low Voltage Applications” **SRC TECHCON**, November 2008 (Best paper in session Award)

C55. **J. P. Kulkarni**, K. Kim and K. Roy, "A 160mV Fully Differential Robust Schmitt Trigger based Sub-threshold SRAM” **SRC TECHCON** 2007

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