VIVEK P. TELANG

Education

Ph.D., Dept. of Electrical Eng., University of Notre Dame, May 1991
Dissertation: *Error-Control Coding for the N-User Multiple Access Channel.*
M.S., Dept. of Electrical Eng., University of Notre Dame, December 1984
B.Tech., Dept. of Electrical Eng., Indian Institute of Technology, Bombay, India, May 1983.

Experience

9/19-*present*: Lecturer, Dept of ECE, University of Texas at Austin

Classes taught:

- Spring 2020 – EE351K Probability and Random Processes
- Fall 2019 – EE362K Introduction to Automatic Control

9/04-*present*: Broadcom Limited, Austin TX

Vice President, Engineering, Physical Layer Products (3/15-present)
Senior Director of Engineering, Physical Layer Products (3/10-3/15)
Director of Engineering, Physical Layer Products (9/04-3/10)
Responsibilities include:

- System-level architecture and signal processing for all physical layer products from 100Mbit/s to 100Gbit/s over optical fiber, copper cable and backplanes
- Annual product revenue > $800M
- Managing a ~200-member engineering organization with more than 30 Ph.Ds
- Management of ASIC engineering functions
  - SerDes IP development and management for 8 Business Units across Broadcom
  - IC development for SerDes transceivers for optical fiber and copper cable
  - High-speed (~50GHz) PCB Board design and Signal Integrity
  - Software development for Automotive PHY and Power-over-Ethernet devices
  - Firmware development for high-speed copper and optical fiber PHYs
- Individual Contributor on system-level architecture design and simulation of 10G, 25G, 50G and 100G PAM4 SerDes Transceivers (15 patents)
- Representative at IEEE 802.3 and OIF standards bodies (2004-2010)
- Customer liaison for all advanced technology engagements

7/99-9/04: Cicada Semiconductor (acquired by Vitesse), Austin TX

Design Manager, Gigabit Ethernet

- Responsible for the system-level IC architecture design, development, simulation and testing of Gigabit Ethernet (10/100/1000BASE-T) PHY layer Transceivers. System Architect, Project Lead, Lead DSP Designer, Responsible for Lab Characterization, Debug and Functional Validation Lead, UNH Compliance Testing, Interoperability Testing, Competitive Analysis, Statistical Lab Qualification and Marketing Collateral (White papers, Power Point slides).
- Directed the design and development efforts of 5-8 members of technical staff. Responsible for overall project management as well as the direction of day-to-day development activities.
- Methodology Improvement - Digital Verification, Lab Characterization
- External Liaison to customers, IEEE 802.3 standards

9/95-9/99: Cirrus Logic, Austin, TX

Project Manager, Communications Division (6/97-9/99)
Design Engineer, Communications Division (9/95-6/97)

- Responsible for the system-level IC architecture design, development, simulation and testing of the PHY layer of Fast Ethernet (100Mbps) transceivers.
- System-level investigation and architecture definition for Gigabit Ethernet, ADSL and HDSL2 transceivers.

3/85-9/95: Tellabs Research Center, Mishawaka, Indiana
Research Engineer

- Conducted self-directed research and designed prototypes for various network access and data transmission products (HDSL, Data Compression, ADPCM codec, ATM, BISDN)
- Directed the research and development efforts of 2-3 members of research staff.

Areas of Technology Expertise

- **100G PAM4, 50G PAM4, 25G and 10G Serdes for optical and copper channels** System-level design and simulation of SerDes transmitters and receivers based on analog signal processing (continuous time filters) as well as digitally implemented FFE/DFE architectures (2004-present)
- **10G Ethernet (10GBASE-T), Gigabit (1000BASE-T) Ethernet and Fast Ethernet (100BASE-TX, 100BASE-T2) Transceivers over twisted pair copper cables:** System-level IC design and development of the PHY layer of a 1000BASE-T transceiver. System-level IC design and development of the PHY layer of a 100BASE-T2 transceiver. System-level IC design and development of the PHY layer of a 100BASE-TX transceiver, particularly the analog adaptive equalizer and PLL. Actively involved in the development of the IEEE 802.3 10GBASE-T standards. (1995-97)
- **Digital Subscriber Loop (HDSL, HDSL2 and ADSL) Transceivers:** Designed and developed a high-level algorithmic simulation as well as a VLSI Implementation of an HDSL Transceiver capable of T1 rate (1.544 Mbit/s) communication over two copper twisted-pairs. Designed and developed a high-level algorithmic simulation of an HDSL2 Transceiver capable of T1 rate (1.544 Mbit/s) communication over a single copper twisted-pair. Analytical study and architecture definition of an ADSL transceiver. (1990-93, 97-99)
- **Cable Modem for Telephony and Data Transmission over CATV Networks:** Design and development of a burst-mode QAM modem to implement multipoint-to-point data transmission. Conducted an analytical comparative study of CDMA, TDMA, FDMA and DMT. Design and development of a multiple access algorithm to implement data transmission over a coaxial CATV network. (1993-95)
- **Traffic Management and Congestion Control for Broadband ISDN Networks:** Analysis of traffic patterns in a high-speed network, and investigation of resource allocation techniques to control congestion. Actively involved in the development of B-ISDN standards by T1S1 and CCITT Standards Bodies. (1989-92)
- **Forward Error Correction (FEC) for Multi-User Systems (Ph.D. Dissertation):** Analysis of Multi-User System characteristics and efficiency. Designed an N-user Multiple-Access System with variable error control, using Reed-Solomon Block codes as well as Convolutional codes, with error control inversely proportional to N, the number of users. (1989-91)
- **Spectrally-shaped Line Codes (Ph.D. Research):** Analysis of desirable spectral characteristics achievable through line coding. Designed an error-correcting line code with desirable spectral parameters and a substantial improvement in efficiency compared to known line codes. (1986-89)
- **Data Compression (Ph.D. Research):** Analysis of noiseless data compression algorithms; Designed and developed a high-level algorithmic simulation of a noiseless 2:1 Data Compaction algorithm. (1988-89)
- **Voice-band Data Transmission:** Designed and developed a high-level algorithmic simulation as well as a real-time microprocessor-based implementation of a voice-band modem capable of full-duplex data transfer at 1200 bit/s using only the lower half of the telephone bandwidth. (1987-88)
- **Speech Activity Analysis (M.S. Research):** Analysis of speech patterns; Designed and developed a high-level algorithmic simulation and a real-time microprocessor-based implementation of a speech activity detector as part of a Digital Speech Interpolation (DSI) system. (1984-86)

- **Integrated Services Digital Networks (ISDN):**
  Studied theory and applications related to ISDN technology, particularly the user-specific U-interface (1986-87)
- **DSP Applications:**
  Designed and implemented real-time implementations of a variety of tone detection algorithms for disabling Echo Cancellers, DTMF systems, ADPCM speech coding, etc.

Areas of Academic Expertise

Communication Theory
Digital Signal Processing
Stochastic Processes
Information Theory
Linear Systems
Coding Theory
Control Systems

Presentation /Teaching Highlights

- Taught Graduate level courses on Advanced Digital Communication Theory (Lee & Messerschmitt) at Cirrus Logic (1998) and Tellabs Research Center (1994)
- Dell CTO Workshop (2017)
- ZTE CTO Workshop (2016)
- ISSCC 2012 Panel Speaker: *10-40 Gb/s I/O Design for Data Communications*
- Broadcom Technical Conference and Technical Seminar (2010, 2011, 2016)
- Technical Seminar at IEEE Denver Section: "*Equalization for High-Speed Serdes Systems – A System-level Comparison of Analog and Digital Techniques"*, 2012.
- Broadcom Worldwide Sales Conference (2006, 2007)

Skills

- **Programming:** MATLAB, C
- **IC Design Tools:** Analog Artist (Cadence), Design Compiler (Synopsys), HSpice, ncVerilog (Ambit).
- **Project Management Tools:** MS Project, JIRA, Bugzilla, Dotproject

Publications and Patents

- **Journals:** IEEE Transactions on Information Theory (1988, 1998)
- **Conference Proceedings:** ICC '96, ISIT '90, Allerton '87, '88, '90, '93, CISS '87, SPIE '87, IWIT '88
- **Standards Contributions:** T1S1 (1990), IEEE 802.3 (1996-97, 2000-2010)
- **Patents:** 16 granted

Other

- U.S. Citizen