Andreas Gerstlauer

Curriculum Vitae

Department of Electrical and Computer Engineering
University of Texas at Austin
2501 Speedway, Stop C0803
Austin, TX 78712, USA
Phone: +1 (512) 232-8294 Fax: +1 (512) 471-8967
gerstl@ece.utexas.edu http://www.ece.utexas.edu/~gerstl/

January 2020

EDUCATION

4 / 2004 University of California, Irvine — Irvine, CA
Ph.D., Information and Computer Science
Thesis title: *Modeling Flow for Automated System Design and Exploration*
Advisor: Prof. Daniel D. Gajski

9 / 1998 University of California, Irvine — Irvine, CA
M.S., Information and Computer Science

5 / 1997 University of Stuttgart — Stuttgart, Germany
Diplom-Ingenieur (M.S.), Electrical Engineering
Thesis title: *Development of a Standard Cell Library in CMOS and Pass Transistor Logic for Low Power Applications*

10 / 1991 University of Stuttgart — Stuttgart, Germany
Vordiplom (B.S.), Electrical Engineering

EXPERIENCE

Academic

1/2017-6/2017 Electrical and Computer Engineering — Technical University of Munich (TUM), Munich, Germany
Visiting Professor

- Researched host-compiled simulation technology and soft-error reliability modeling in collaboration with Prof. U. Schlichtmann, Chair of Electronic Design Automation (EDA).

9/2016-12/2016 Computer Science — Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany
Visiting Professor

- Researched application of approximate computing principles in the context of circuit reliability under aging, temperature and other degradations in collaboration with Prof. J. Henkel, Chair of Embedded Systems (CES).

9/2014-present Electrical and Computer Engineering — University of Texas, Austin, TX
Associate Professor

- Researched network-level modeling, design and design automation methods for cyber-physical networks-of-systems (CPNoS).
- Researched heterogeneous, accelerator-rich compute platforms for high-performance, scientific computing applications.
- Researched system-level performance, energy, reliability, power and thermal (PERPT) modeling techniques for heterogeneous multi- and many-cores (in collaboration with Prof. John).
- Researched power-aware compilation, approximation and runtime management concepts for energy-smart system-on-chip (SoC) design and operation (in collaboration with Prof. John)

8/2008-8/2014 Electrical and Computer Engineering — University of Texas
Assistant Professor — Austin, TX

- Researched host-compiled simulation technology for electronic-system level (ESL) modeling, synthesis and design space exploration.
- Researched heterogeneous computing platforms and novel accelerator designs for linear algebra processing (in collaboration with Prof. van de Geijn) and for stochastic simulation of biological networks (in collaboration with Profs. Vikalo).
- Researched approximate computing techniques for ultra low-power circuit operation (in collaboration with Prof. Orshansky).

5/2004-7/2008 Center for Embedded Computer Systems — University of California
Assistant Researcher — Irvine, CA

- Researched and developed electronic system-level (ESL) design automation (EDA) tools for synthesis of multi-processor and multi-core system platforms and SoC/NoC communication architectures.
- Successfully transferred Specify-Explore-Refine (SER) technology for adoption by the Japanese Aerospace Exploration Agency (JAXA), NEC Toshiba Space Systems and general commercial availability.
- Managed, led and co-supervised research project in team of 5-10 post-doctoral researchers, project scientists and project staff.
- Interfaced with sponsors and partners in Japan on project requirements, deliverables and commercialization.

1998-2004 Center for Embedded Computer Systems — University of California
Graduate Research Assistant — Irvine, CA

- Researched and developed a complete, automated SoC Design Environment (SCE) for synthesis of abstract system specifications down to optimized hardware/software (RTL/ISS) implementations.
- Researched system-level design models and the SpecC system design methodology in contracts with the Semiconductor Research Cooperation (SRC) and industry sponsors.
- Co-supervised and led research and development team of 5-10 students, visiting researchers and developers.
- Implemented several embedded system designs and system-on-chip (SoC) applications in contracts with Motorola and Conexant.

1996-1997 Integrated Systems Engineering Group — University of Stuttgart
Graduate Research Assistant — Stuttgart, Germany

- Investigated different logic families for use with a new semiconductor technology (three-dimensional silicon-on-insulator (SOI) process).
- Developed a standard cell library in Double Pass-Transistor Logic (DPL) and standard static CMOS logic. Implemented various designs in both logic styles.

1995-1996 Institute for Microelectronics Stuttgart — University of Stuttgart
Research Assistant — Stuttgart, Germany

- Researched and developed a synthesizable RISC micro-controller core in VHDL.
- Synthesized, simulated and verified the design using industry-standard design flows.

1993-1994 Institute of Comm. Networks & Comp. Eng. — University of Stuttgart
Research Assistant — Stuttgart, Germany

- Simulation of different permit distribution protocols for a permit-based fiber-to-the-home (FTTH) ATM access network.
- Queuing theory based statistical analysis for different traffic scenarios.

Teaching

4/2017-6/2017 Electrical and Computer Engineering — Technical University of Munich (TUM), Munich, Germany
Visiting Professor

- Taught graduate class on "Advanced Topics in IC Design: Embedded System Design and Modeling" (SS'17) in international Master of Science in Communications Engineering (MSCE) program.

9/2014-present Electrical and Computer Engineering — University of Texas, Austin, TX
Associate Professor

- Updated and taught graduate class on "Embedded System Design and Modeling" (EE382N.23: F'15, F'17). Average instructor rating of 4.6/5.0.
- Updated and taught graduate class on "System-on-Chip Design" (EE382M.20: F'14, F'18). Average instructor rating of 4.5/5.0.
- Adopted, revamped and taught cross-listed upper-division undergraduate/graduate class on "Real-Time Systems/Real-Time Operating Systems" (EE445M/EE380L.6: S'15, S'16, S'18). Average instructor rating of 4.6/5.0.

8/2008-8/2014 Electrical and Computer Engineering — University of Texas, Austin, TX
Assistant Professor

- Adopted and revamped graduate class on "System-on-Chip Design" (EE382V: S'10, S'11, F'12). Average instruction rating of 4.3/5.
- Taught lower-division undergraduate class on the first "Introduction to Embedded Systems" (EE319K: S'09, S'11, S'12, S'13, F'13). Average instructor rating of 4.1/5.
- Developed new introductory graduate class on "Embedded System Design and Modeling" (EE382V: F'08, F'09, F'10, F'11). Average instructor rating of 4.2/5.

2005-2008 Electrical Engineering and Computer Science — University of California, Irvine, CA
Lecturer

- Instructor on record for undergraduate class in digital logic design (EECS/CSE 31, "Introduction to Digital Systems," F'07). Instructor rating of 3.06/4.
- Taught lectures for undergraduate class in digital logic/system design (EECS/CSE 31).
- Taught lectures for graduate class on SoC design and exploration (EECS 221).

2002 Information and Computer Science — University of California, Irvine, CA
Teaching Assistant

- Provided assignments and guided students for advanced graduate seminar in system design (ICS 259, W'02).

1997-1998 Information and Computer Science — University of California, Irvine, CA
Teaching Assistant

- Developed and guided lab projects for senior undergraduate computer design laboratory class (ICS 155B, S'98).
- Developed and guided lab projects for senior undergraduate logic design laboratory class (ICS 155A, W'98).
- Designed and graded exams and taught discussion sections for senior undergraduate class in computer networks (ICS 153, F'97).

Industry

1989-1997 Ehrler Prüftechnik — Steinenbronn, Germany
Senior Software Engineer, Project Manager

- Developed real-time software for process control, automation, data acquisition, and data analysis in complex industrial test benches for automotive applications.
- Managed and led projects with team of 2-5 programmers. Coordinated software

development/testing with electromechanical design teams.

- Documented and negotiated software requirements specifications with various clients. Developed contracts and product documentation.
- Supervised, coordinated and performed deployment, installation and maintenance of testbench software at client sites in Europe and USA.

1994 Böblingen Instruments Division (BID) — Hewlett-Packard GmbH, Böblingen, Germany
Summer Intern

- Designed and implemented a C++ sub-process for printing in an optical time-domain reflectometer (OTDR) measurement instrument.

HONORS AND AWARDS

2017	TUM-IAS Visiting Fellow	Technical University of Munich, Institute for Advanced Studies, Germany
2016	Best in Session Award at SRC TECHCON (with student Xinnian Zheng and Prof. Lizy K. John)	Semiconductor Research Corporation (SRC)
2016-2017	Humboldt Research Fellowship for Experienced Researchers	Alexander von Humboldt Foundation, Germany
2015	Best Research Paper Award (with student Xinnian Zheng and Prof. Lizy K. John) at the 52nd Design Automation Conference (DAC)	Design Automation Conference (DAC)
2015	Best Paper Award (with student Xinnian Zheng and Profs. Pradeep Ravikumar and Lizy K. John) at the 15th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)	SAMOS XV Conference
2013	Best in Session Award at SRC TECHCON (with students Zhuoran Zhao and Suhas Chakravarty)	Semiconductor Research Corporation (SRC)
2013	Best Poster Award for student Ardavan Pedram at the International Parallel & Distributed Processing Symposium (IPDPS) Ph.D. forum	IEEE Computer Society Technical Committee on Parallel Processing
2011	Senior Member	IEEE
2010-2014	AMD Chair in Computer Engineering	Advanced Micro Devices
2008	OS Modeling Paper Selected as One of the Most Influential Contributions in 10 Years at DATE	Design, Automation and Test in Europe Conference (DATE)
2003	Travel grant	ACM SIGDA
2002	Young Student Mentor	Design Automation Conference (DAC)
2000-2001	Motorola Research Fellow	Motorola, Inc.
1998	Professional Development Award	Design Automation Conference (DAC)
1998	Advanced Study Institute Grant	NATO ASI
1997	Graduated *summa cum laude* (“*mit Auszeichnung*”)	University of Stuttgart, Germany

MEMBERSHIPS IN PROFESSIONAL SOCIETIES

1997-present Institute of Electrical and Electronics Engineers (IEEE)
- Circuits & Systems Society (CAS)
- Computer Society (CS)
- Council on Electronic Design Automation (CEDA)

2003-present Association of Computing Machines (ACM)
- Special Interest Group on Design Automation (SIGDA)
- Special Interest Group on Embedded Systems (SIGBED)

PROFESSIONAL SERVICE

University Committees

2015-present Member, Curriculum Committee, ECE Dept., UT Austin

2015-present Curriculum Coordinator and Chair, Integrated Circuits and Systems/Electronics and Integrated Circuits (ICS/EIC) Curriculum Committee, ECE Dept., UT Austin

2014-2015 Member, Software Engineering Lecturer Search Committee, ECE Dept., UT Austin

2013-2016 Member, Silicon Labs Endowed Chair Search Committee, ECE Dept., UT Austin

2012-2013 Chair, Computer Architecture and Embedded Processors (CAEP) Graduate Admissions Committee, ECE Dept., UT Austin

2010 Member, Faculty Search Committee, ECE Dept., UT Austin

2009-2012 Chair, Integrated Circuits and Systems (ICS) Prospective Graduate Student Site Visit Committee, ECE Dept., UT Austin

2009-present Member, Computer Architecture and Embedded Processors (CAEP)/Architecture, Computer Systems, and Embedded Systems (ACSES) Graduate Admissions Committee, ECE Dept., UT Austin

2009-present Member, Computer Architecture and Embedded Processors (CAEP)/Architecture, Computer Systems, and Embedded Systems (ACSES) Curriculum Committee, ECE Dept., UT Austin

2009-present Member, Computer Architecture and Embedded Processors (CAEP)/Architecture, Computer Systems, and Embedded Systems (ACSES) Faculty Committee, ECE Dept., UT Austin

2008-2013 Member, Computer Engineering (CE) Graduate Admissions Committee, ECE Dept., UT Austin

2008-2013 Member, Computer Engineering (CE) Curriculum Committee, ECE Dept., UT Austin

2008-2013 Member, Computer Engineering (CE) Faculty Committee, ECE Dept., UT Austin

2008-present Member, Integrated Circuits and Systems (ICS) Graduate Admissions Committee, ECE Dept., UT Austin

2008-present Member, Integrated Circuits and Systems/Electronics and Integrated Circuits (ICS/EIC) Curriculum Committee, ECE Dept., UT Austin

2008-present Member, Integrated Circuits and Systems/Electronics and Integrated Circuits (ICS/EIC) Faculty Committee, ECE Dept., UT Austin

2008-present Member, Graduate Studies Committee (GSC), ECE Dept., UT Austin

Outside Committees

2014-present	Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES)
2013-present	Associate Editor, ACM Transactions on Embedded Computing Systems (TECS)
2021	General Chair, ACM/IEEE Embedded Systems Week (ESWEEK)
2020	General Co-Chair, ACM/IEEE Embedded Systems Week (ESWEEK)
2020	Member, Technical Program Committee, ACM/EDAC/IEEE Design Automation Conference (DAC)
2020	Member, Technical Program Committee, Design, Automation and Test in Europe (DATE) Conference
2019	Tutorials and Special Sessions Chair, ACM/IEEE Embedded Systems Week (ESWEEK)
2018	Tutorial Chair, ACM/IEEE Embedded Systems Week (ESWEEK)
2018	Member, Technical Program Committee, ACM/EDAC/IEEE Design Automation Conference (DAC)
2018-2019	Member, Technical Program Committee, ACM Workshop on Software and Compilers for Embedded Systems (SCOPES)
2017-2018	Co-Chair, Topic D1 “System Specification and Modelling”, Design, Automation and Test in Europe (DATE) Conference
2017-2019	Member, Technical Program Committee, IEEE/ACM/IFIP International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)
2017-2019	Member, Technical Program Committee, ACM International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation (SAMOS)
2016	Guest Editor, International Journal of Parallel Programming (IJPP), Special Issue on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XV)
2016	Chair, Technical Program Committee, IEEE/ACM/IFIP International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)
2016	Chair, Technical Program Committee, IEEE International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation (SAMOS)
2016, 2019	Member, Technical Program Committee, Workshop on Approximate Computing Across the Stack (WAX)
2016	Member, Technical Program Committee, International Conference on VLSI Design and International Conference on Embedded Systems (VLSI)
2006-2016	Member, Technical Program Committee, Design, Automation and Test in Europe (DATE) Conference
2015-2016	Editor, Section on “Codesign Tools and Environments”, Handbook of Hardware/Software Codesign (edited by Soonhoi Ha and Jürgen Teich), Springer
2015	General and Finance Chair, ACM/IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE)
2015	Co-Chair, Technical Program Committee IEEE/ACM/IFIP International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)

2015	Chair, Track "Modeling, Design, and Design Space Exploration", IEEE International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation (SAMOS)
2015	Member, Technical Program Committee, 1st International ESWEEK Workshop on Resiliency in Embedded Electronic Systems (REES)
2007-2015, 2019	Member, Technical Program Committee, International Embedded Systems Symposium (IESS)
2012-2015	Associate Editor, Springer Design Automation for Embedded Systems (DAEM) Journal
2012-2015	Chair, Subcommittee EDA1 "System-Level Design and Codesign", ACM/EDAC/IEEE Design Automation Conference (DAC)
2012-2015	Member, Technical Program Committee, Electronic System Level Synthesis Conference (ESLsyn)
2014-2015	Member, Technical Program Committee, IEEE International Conference on Reconfigurable Computing and FPGA (ReConfig)
2014	Chair, Track 4 "Embedded System Architecture", IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2014	Member, Technical Program Committee, IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
2014	Member, Technical Program Committee, IEEE Conference on Design and Architectures for Signal and Image Processing (DASIP)
2014	Member, Technical Program Committee, IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)
2014	Member, Technical Program Committee, IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC)
2014	Member, Technical Program Committee, IFIP Workshop on Software Technologies for Future Embedded and Ubiquitous Systems (SEUS)
2009-2014	Member, Technical Program Committee, IEEE/ACM/IFIP International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)
2010-2014	Member, Technical Program Committee, IEEE International Conference on Computer Design (ICCD)
2013	Member, Program Committee, ACM SIGDA Student Research Competition (SRC) at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
2013	Chair, Technical Area "Architecture and Implementation", Asilomar Conference on Systems, Signals and Computers (ACSSC)
2013	Co-Chair, Track T8 "Embedded Systems/HW-SW Codesign/Logic & High Level Synthesis", IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)
2013	Co-Chair, Technical Program Committee, Electronic System Level Synthesis Conference (ESLsyn)
2012	Co-Chair, Track T11 "Logic and high-level synthesis, SW synthesis, HW-SW co-design", IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)
2011	Registration Chair, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)

2009, 2011	Member, Technical Program Committee, International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)
2010	Co-organizer, Workshop on Compiler-Assisted System-On-Chip Assembly (CASA)
2010	Member, Technical Program Committee, IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Work-in-Progress (WiP) Track
2010	Chair, Technical Program Committee (TPC), Austin Conference on Integrated Systems and Circuits (ACISC)
2008-2010	Member, Technical Program Committee, International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS)
2009-2010	Chair, Topic "Hardware/Software Codesign", IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2009	Tutorial Chair, Austin Conference on Integrated Systems and Circuits (ACISC)
2009	Member, Technical Program Committee, Austin Conference on Integrated Systems and Circuits (ACISC)
2008	Member, Technical Program Committee, International Conference on Embedded Systems and Critical Applications (ICESCA)
2007	Local Arrangements Chair, International Embedded Systems Symposium (IESS)

Conference Service

2020	Co-Organizer, Dagstuhl Seminar 20222 "Approximate Systems", Schloss Dagstuhl – Leibniz Zentrum für Informatik, Wadern, Germany.
2019	Session Co-Chair, ACM/EDAC/IEEE Design Automation Conference (DAC)
2017-2018	Co-Organizer (with A. Shrivastava), ACM/IEEE Early Career Workshop, ACM/EDAC/IEEE Design Automation Conference (DAC)
2015	Session Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
2014	Session Chair, Virtual Prototyping of Parallel and Embedded Systems (ViPES) Workshop, Special Session at the 21st IEEE Reconfigurable Architectures Workshop (RAW)
2013	Organizer and Moderator, Industry Panel on "System-Level Design and High-Level Synthesis", IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2013	Session Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2011	Session Chair, ACM/EDAC/IEEE Design Automation Conference (DAC)
2011	Co-Organizer (with C. Haubelt), Special Session on "Embedded Multi-Processor Software Synthesis", ACM/EDAC/IEEE Design Automation Conference (DAC)
2010	Co-Organizer (with R. Dömer), Designer Forum session on "Embedded Software Development for Multi-Processor System-on-Chip", IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)
2009	Session Chair, International Embedded Systems Symposium (IESS)
2009	Session Co-Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)

2009	Session Chair, "Automating Model Generation and Implementation", Design, Automation and Test in Europe (DATE) Conference
2009	Co-Organizer (with R. Dömer, W. Mueller), Special Session on "Hardware Dependent Software for Multi-Core Embedded Systems", IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)
2007	Session Chair, International Embedded Systems Symposium (IESS)
2007	Organizer, Center for Embedded Computer Systems (CECS) booth, ACM/IEEE Design Automation Conference (DAC)
2006	Session Co-Chair, Design, Automation and Test in Europe (DATE) Conference

Reviewer

2011, 2014	ACM Journal of Emerging Technologies in Computing (JETC)
2008, 2011-14	ACM Transactions on Design Automation of Electronic Systems (TODAES)
2009-17	ACM Transactions on Embedded Computing Systems (TECS)
2012, 2015	IEEE Computer Architecture Letters (CAL)
1999, 2010	IEEE Design & Test of Computers (D&T) Magazine
2009-10	IEEE Embedded System Letters (ESL)
2013-15, 2018	IEEE Micro
2000, 2005	IEEE Transaction on VLSI Systems (TVLSI)
2004, 2010, 2014-17	IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)
2013-14, 2016-18	IEEE Transactions on Computers (TC)
2015-16	IEEE Transactions on Emerging Topics in Computing (TETC)
2009-10	IEEE Transactions on Industrial Informatics (TII)
2012	IEEE Transactions on Multimedia (TMM)
2018-2019	IEEE Transactions on Sensor Networks (TOSN)
2018	IEEE Transactions on Sustainable Computing (TSUSC)
2012	Elsevier Embedded Hardware Design (Microprocessors and Microsystems)
2017	Elsevier Integration, the VLSI Journal
2005, 2008-10	Elsevier Journal of Systems Architecture (JSA)
2007	EURASIP Journal of Embedded Systems (JES)
2002	Journal for Circuits, Systems and Computers (JCSC)
2015	Science China Information Sciences (SCIS)
2006, 2012, 2018	Springer Design Automation for Embedded Systems (DAEM) Journal
2017	Springer Journal of Signal Processing Systems (JSPS)
1998-2011	ACM/IEEE Design Automation Conference (DAC)
1999, 2002	Design, Automation and Test in Europe (DATE) Conference

2002-03	IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)
2003-04	IEEE/ACM/IFIP International Conference on Hardware/Software Co-design and System Synthesis (CODES+ISSS)
1998	International Symposium on System Synthesis (ISSS)

Other Service

2013, 2018, 2019 (2x)	Panel Reviewer, National Science Foundation (NSF)

FUNDING

Grants and Contracts

9/2019-8/2021	"Novel Computing Paradigms for Partial Differential Equations," PI (with L. K. John), Sponsored Research Agreement UTA19-000749, $488,375 (my share: $232,712)	ExxonMobil Research and Engineering
7/2019-7/2020	"Power Bander Evaluation," Subcontract with Applied Research Laboratories (ARL:UT) as PIs (with M. Orshansky and M. Tiwari), Sponsored Research Agreement, $282,000 (UT ECE share: $140,000, my share: $46,607)	Marine Corps Warfighting Laboratory (MCWL)
7/2019-6/2023	"SHF: Medium: Simulation-Based Analysis of EM Side Channels in Embedded Systems: From Software to Fields," (with M. Orshansky, PI, and A. Yilmaz), Grant CCF-1901446, $1,200,000 (my share: $400,000).	National Science Foundation (NSF)
1/2019-1/2020	"Learning-Based Performance, Power and Thermal Prediction," PI (with L. K. John, Co-PI), Sponsored Research Agreement UTA17-001153, $99,929 (my share: $90,429).	Samsung Global Research Outreach (GRO) Program
10/2018-9/2021	"SHF: Medium: Collaborative Research: Predictive Modeling for Next-generation Heterogeneous System Design," PI (with L. K. John and P. Brisk, UC Riverside), Grant CCF-1763848, $1,001,941 (UT Austin share: $679,411, my share: $339,706).	National Science Foundation (NSF)
Awarded 2017[1]	"Automatic Synthesis of Proxies for Emerging Workloads and Systems," Co-PI (with L. K. John, PI), Task ID 2806.001, $210,000 (my share: $105,000).	Semiconductor Research Corporation (SRC)
10/2017-9/2020	"SPX: CISIT: Computing In Situ and In Memory for Hierarchical Numerical Algorithms," Grant CCF-1725743, Co-PI (with G. Biros, PI, and L. K. John), $800,000 (my share: $270,621).	National Science Foundation (NSF)
10/2016-1/2020	"Cyber Security Research on Power Models," Co-PI (with M. Tiwari, PI, and M. Orshansky), Sponsored Research Agreement RPP001-MRA16-005, $750,000 (my share: $199,790).	Lockheed Martin Corporation (LMC)

[1] Selected for funding by SRC, but cancelled due to contract language discussions between UT Austin and SRC not reaching a timely agreement on SRC's new 2018 terms.

9/2015-12/2016	"Scalable Network/System Co-Simulation For Power and Performance Aware Network-of-Systems Design," PI (with L. K. John, Co-PI), Sponsored Research Agreement UTA15-000880, $99,985 (my share: $49,993).	Samsung Global Research Outreach (GRO) Program
9/2015-1/2017	"Adaptive Energy-Efficient Designs for Next Generation Smart Phone CPUs," Co-PI (with L. K. John, PI), Sponsored Research Agreement UTA15-000885, $99,985 (my share: $49,993).	Samsung Global Research Outreach (GRO) Program
10/2014-9/2018	"CSR: Small: Network-Level Design of Cyber-Physical Systems," PI, Grant CNS-1421642, $488,281.	National Science Foundation (NSF)
9/2013-8/2017	"XPS: DSD: A2MA - Algorithms and Architectures for Multiresolution Applications," Co-PI (with G. Biros, PI, L. K. John, and R. van de Geijn, CS), Grant CCF-1337393, $749,801 (my share: $221,246).	National Science Foundation (NSF)
6/2013-12/2013	"Core Technology Development for System Simulation including Network," PI, Sponsored Research Agreement UTA12-001141, $149,020.	Samsung Electronics Co., DMC R&D Center, Korea
8/2012-7/2013	"Automated Design Space Exploration and Optimization of DSP Systems," PI, Sponsored Research Agreement UTA12-000636, $60,000	National Instruments, Austin, TX
9/2012-8/2013	"Interference Alignment in Distributed Environments," co-PI (with R. W. Heath, PI), $99,980 (my share: $49,990).	Army Research Office (ARO)
8/2012-5/2016	"Multi-dimensional Modeling, Design and Exploration of Heterogeneous Multicore SoCs," PI (with L. K. John), Task ID 2317.001, Contract 2012-HJ-2317, $345,000 (my share: $173,000).	Semiconductor Research Corporation (SRC)
6/2012-5/2017	"SHF: Small: Algorithm/Architecture Co-Design of Low Power and High Performance Linear Algebra Compute Fabrics," PI (with R. van de Geijn, CS), Grant CCF-1218483, $499,919 (my share: $249,960).	National Science Foundation (NSF)
9/2011-5/2012	"Interference Alignment for Wireless Network after Next (WNaN)," co-PI (with R. W. Heath, PI), $99,344 (my share: $49,672).	Defense Advanced Research Projects Agency (DARPA)
2011	"Towards Enabling Full−Cell Biochemical Network Simulations," Summer Research Assignment (SRA), $20,000.	Graduate School, UT Austin
9/2010-8/2015	"SHF: Small: Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance," PI (with M. Orshansky), Grant CCF-1018075, $449,676 (my share: $224,807).	National Science Foundation (NSF)
8/2010-1/2015	"Automatic Platform Model Calibration and Tuning," PI, Task ID 2085.001, Contract 2010-HJ-2085, $255,000.	Semiconductor Research Corporation (SRC)
2006-2008	"SER Upgrades and Extensions," Co-PI (with D. Gajski, PI), Research Grant, ¥163,000,000 ($1,390,000, my share: $695,000).	InterDesign Technologies, Inc., Japan

Gifts

2019	"Scheduling and Virtualization for Extremely Heterogeneous Systems with Hardware Threads for Near-Memory Computing", unrestricted research gift, $50,000.	ARM Research, Austin, TX
2019	"Learning-based Power and Performance Estimation for Heterogeneous HW Platforms", unrestricted research gift, $100,000.	Bosch Research, Renningen, Germany
2017-2018	"UT Lab for Side-Channel Security: Experimental Validation of Embedded System Security against Electromagnetic Side-Channel Attacks," Co-PI (with A. Yilmaz, PI, M. Orshansky, and M. Tiwari), Kilby Award Equipment Grant, $20,000 (my share: $5,000).	Cockrell School of Engineering (CSE), UT Austin
2017-2020	"Miniaturized Proxies of Industry Standard Benchmarks for Pre-silicon Evaluation," Co-PI (with L. K. John, PI), unrestricted research gift, $240,000 (my share: $120,000).	Intel Labs, Santa Clara, CA
2013-2016	"Energy-Smart SoC Rapid Prototyping ISRA: Power-Aware System Compilation," PI (with L. K. John), unrestricted research gift, $300,000 (my share: $150,000).	Intel Strategic Research Alliance (ISRA), University Research Office (URO)
2013-2014	"Models of Computation for Design of Dynamic DSP Systems," PI (with B. Evans), unrestricted research gift, $40,000 (my share: $20,000).	National Instruments, Austin, TX
2011-2012	"Adaptive Hardware/Software Platforms for Mobile Web Browsing," co-PI (with K. Pingali, PI), unrestricted research gift, $80,000 (my share: $40,000).	Qualcomm, Bay Area Research Division (BARD), Santa Clara, CA
2011-2012	"Automated Design Space Exploration and Optimization of DSP Systems," PI, unrestricted, no-overhead gift, $40,000.	National Instruments, Austin, TX
2010-2011	"Compiler-Assisted MPSoC Assembly and Mapping," PI, unrestricted research gift, $46,000.	Intel Labs, Santa Clara, CA
2009	"System-Level and System-on-Chip Design," Equipment Grant, $28,678.	Intel Higher Education Program, Portland, OR

In-Kind Donations

2010, 2013, 2014	Prototyping boards and software licenses for SoC teaching lab, $12,670	Xilinx, Inc., San Jose, CA
2011	Test and measurement equipment (logic analyzers, function generators, oscilloscopes) for Digital Integrated Circuits and Systems lab, $300,659	Dell, Inc., Round Rock, TX

ADVISING AND SUPERVISION

Ph.D. Dissertations Supervised

13. Zhuoran Zhao, "Network-Level Design Space Exploration of Resource-Constrained Networks-of-Systems," Electrical and Computer Engineering, The University of Texas at Austin, April 26, 2019. (supervisor)
12. Wooseok Lee, "User-aware Performance and Energy Management for Interactive, Multi-tasking Mobile Systems," Electrical and Computer Engineering, The University of Texas at Austin, March 13, 2019. (supervisor, co-supervisor with Prof. L. K. John)

11. Seogoo Lee, "Approximate High-Level Synthesis of Quality and Energy Optimized Hardware Processors," Electrical and Computer Engineering, The University of Texas at Austin, August 25, 2017. (supervisor)
10. Xinnian Zheng, "Learning-Based Analytical Cross-Platform Performance and Power Prediction," Electrical and Computer Engineering, The University of Texas at Austin, April 19, 2017. (supervisor, with co-supervisor Prof. L. K. John)
9. Dongwook Lee, "Learning-Based System-Level Power Modeling of Hardware IPs," Electrical and Computer Engineering, The University of Texas at Austin, April 19, 2017. (supervisor)
8. Jin Miao, "Modeling and Synthesis of Approximate Digital Circuits," Electrical and Computer Engineering, The University of Texas at Austin, November 11, 2014. (co-supervisor with Prof. M. Orshansky)
7. Parisa Razaghi, "Dynamic Time Management for Improved Accuracy and Speed in Host-Compiled Multi-Core Platform Models," Electrical and Computer Engineering, The University of Texas at Austin, April 21, 2014. (supervisor)
6. Dylan Pfeifer, "Parallel and Distributed Cyber-Physical System Simulation," Electrical and Computer Engineering, The University of Texas at Austin, December 2, 2013. (co-supervisor with Prof. J. Valvano)
5. Ardavan Pedram, "Algorithm/Architecture Codesign of Low Power and High Performance Linear Algebra Compute Fabrics," Electrical and Computer Engineering, The University of Texas at Austin, July 29, 2013. (supervisor, with co-supervisor Prof. R. van de Geijn, Computer Science)
4. Ku He, "Adaptive Low-Energy Techniques in Memory and Digital Signal Processing Design," Electrical and Computer Engineering, The University of Texas at Austin, April 18, 2012. (co-supervisor with Prof. M. Orshansky)
3. Ahmed Abdel Hadi, "Multicast Networks: Capacity, Algorithms and Implementation," Electrical and Computer Engineering, The University of Texas at Austin, October 17, 2011. (co-supervisor with Prof. S. Vishwanath)
2. Martha Salome Lopez De La Fuente, "Definition, Design and Implementation of a Processor-Based Stimulation System for Electrokinetically-Driven Fluidic Devices," Information Technologies and Communications, Monterey Institute of Technology, Monterey, Mexico, May 11, 2011. (external co-advisor with Prof. S. O. Martinez Chapa)
1. Gunar Schirner, "Improving Accuracy of Transaction Level Models in System-on-Chip Design," Electrical Engineering and Computer Science, University of California, Irvine, March 3, 2008. (co-advisor with Prof. R. Dömer)

Ph.D. Dissertation Committee Member

28. Zheng Xu, "Safe Machine Learning Accelerator and Interconnect Design," Electrical and Computer Engineering, The University of Texas at Austin, August 2, 2019.
27. Shounak Dhar, "Modern FPGA Placement Techniques with Hardware Acceleration," Electrical and Computer Engineering, The University of Texas at Austin, July 24, 2019.
26. Jiajun Wang, "Reuse Aware Data Placement Schemes for Multilevel Cache Hierarchies" Electrical and Computer Engineering, The University of Texas at Austin, April 24, 2019.
25. Hari Angepat, "Logical Partitioning of Parallel System Simulations," Electrical and Computer Engineering, The University of Texas at Austin, October 18, 2018.
24. Yazhou Zhu, "Active Timing Margin Management to Improve Microprocessor Power Efficiency," Electrical and Computer Engineering, The University of Texas at Austin, October 10, 2018.
23. Dan Zhang, "Lightweight Offload Engines for Worklist Management and Worklist-Directed Prefetching," Electrical and Computer Engineering, The University of Texas at Austin, November 28, 2017.

22. Reena Panda, "Accurate Modeling of Core and Memory Locality for Proxy Generation Targeting Emerging Applications and Architectures," Electrical and Computer Engineering, The University of Texas at Austin, November 10, 2017.
21. Xiaoyu Ma "Large-Scale Transactional Execution of FPGA-Accelerated Irregular Applications," Electrical and Computer Engineering, The University of Texas at Austin, April 18, 2017.
20. Nagaraja Revanna, "Memristor Based Arithmetic Circuit Design," Electrical and Computer Engineering, The University of Texas at Austin, November 1, 2016.
19. Subhendu Roy, "Logic and Clock Network Optimization in Nanometer VLSI Circuits," Electrical and Computer Engineering, The University of Texas at Austin, May 5, 2015.
18. Gene Wu, "Performance, Power, and Confidence Modeling of Digital Designs," Electrical and Computer Engineering, The University of Texas at Austin, May 4, 2015.
17. Maysam Lavasani, "Generating Network-attached Accelerators: Methodology and Applications," Electrical and Computer Engineering, The University of Texas at Austin, April 20, 2015.
16. Shahrzad Mirkhani, "Statistical Methods for Rapid System Evaluation under Transient and Permanent Faults," Electrical and Computer Engineering, The University of Texas at Austin, November 24, 2014.
15. Yilin Zhang, "Interconnect Optimizations for Nanometer VLSI Design," Electrical and Computer Engineering, The University of Texas at Austin, June 12, 2014.
14. Mahesh Prabhu, "Scalable Algorithms for Software Based Self Test using Formal Methods," Electrical and Computer Engineering, The University of Texas at Austin, April 24, 2014.
13. Jhih-Rong Gao, "Lithography Aware Physical Design and Layout Optimization for Manufacturability," Electrical and Computer Engineering, The University of Texas at Austin, April 9, 2014.
12. Mark McDermott, "Dataflow Processing Element for a Cognitive Sensor Platform," Electrical and Computer Engineering, The University of Texas at Austin, April 8, 2014.
11. Minsoo Rhu, "Performance-Efficient Mechanisms for Managing Irregularity in Throughput Processors," Electrical and Computer Engineering, The University of Texas at Austin, January 27, 2014.
10. Muhammad Faisal Iqbal, "Workload-Aware Network Processors: Improving Performance While Minimizing Power Consumption," Electrical and Computer Engineering, The University of Texas at Austin, July 16, 2013.
9. Muhammad Tauseef Rab, "Techniques To Minimize Circuitry and Improve Efficiency for Defect Tolerance," Electrical and Computer Engineering, The University of Texas at Austin, April 18, 2013.
8. Jongwook Sohn, "Improved Architectures for Fused Floating-Point Arithmetic Units," Electrical and Computer Engineering, The University of Texas at Austin, March 22, 2013.
7. Evgeni Krimer, "Improving Energy Efficiency of Reliable Massively-Parallel Architectures," Electrical and Computer Engineering, The University of Texas at Austin, April 30, 2012.
6. Alexander Viehl, "Quantitative Synchronisationsanalyse kommunizierender Prozesse zum Echtzeitnachweis verteilter eingebetteter Systeme," Faculty of Science, University of Tubingen, Germany, January 9, 2012.
5. Rudrajit Dutta, "Adaptable and Enhanced Error Correction Codes for Efficient Error and Defect Tolerance in Memories," Electrical and Computer Engineering, The University of Texas at Austin, November 21, 2011.
4. Wooyoung Jang, "Architecture and Physical Design for Advanced Networks-on-Chip," Electrical and Computer Engineering, The University of Texas at Austin, April 25, 2011.
3. Sriram Sambamurthy, "Power Estimation of Microprocessors," Electrical and Computer Engineering, The University of Texas at Austin, May 19, 2010.

2. Henning Zabel, "Techniken zur Simulation von eingebetteten Systemen mit abstrakten RTOS-Modellen," Electrical Engineering, Computer Science and Mathematics, University of Paderborn, Germany, March 19, 2010.
1. Shayak Banerjee, "Enhancing the Design-Manufacturing Interface in Nanoscale Technologies," Electrical and Computer Engineering, The University of Texas at Austin, May 3, 2010.

Ph.D. Qualifying and Candidacy Committee Member

50. Tian Tan, "Tradeoffs Between Soft and Hard Logic," Electrical and Computer Engineering, The University of Texas at Austin, April 29, 2019.
49. Sangkuk Lym, "Memory Bandwidth-Efficient Deep Neural Network Training," Electrical and Computer Engineering, The University of Texas at Austin, March 12, 2019.
48. Sriram Sundaram, "Power Efficient High-Performance CPU and GPU Designs: Power Modeling, Optimization and Verification," Electrical and Computer Engineering, The University of Texas at Austin, November 30, 2018.
47. Zheng Xu, "Fault Resilient System-On-Chip Design," Electrical and Computer Engineering, The University of Texas at Austin, November 20, 2018.
46. Shuang Song, "Improving Graph Processing by Load Balancing and Redundancy Reduction," Electrical and Computer Engineering, The University of Texas at Austin, November 9, 2018.
45. Mochamad Asri, "Hardware-Assisted Data Movement Optimizations for Heterogeneous System Architectures," Electrical and Computer Engineering, The University of Texas at Austin, October 12, 2018. (supervisor)
44. Jiajun Wang, "Data Placement Schemes from Hardware and Software Perspectives," Electrical and Computer Engineering, The University of Texas at Austin, September 27, 2018.
43. Shounak Dhar, "Modern FPGA Placement and Acceleration Techniques," Electrical and Computer Engineering, The University of Texas at Austin, August 29, 2018.
42. Wooseok Lee, "Improving User Experience and Energy Efficiency in Interactive, Multi-tasking Mobile Systems," Electrical and Computer Engineering, The University of Texas at Austin, April 13, 2018. (supervisor)
41. Trenton J. Grale, "Optimizing Elliptic Curve Cryptographic Processors and Their Underlying Modular Arithmetic Functions," Electrical and Computer Engineering, The University of Texas at Austin, March 8, 2018.
40. Song Zhang, "System Resilience for Partitioned Global Address Space," Electrical and Computer Engineering, The University of Texas at Austin, December 10, 2017.
39. Zhuoran Zhao, "Source-Level Network/System Co-Simulation for Design Space Exploration of IoT Applications," Electrical and Computer Engineering, The University of Texas at Austin, October 6, 2017. (supervisor)
38. Yazhou Zu, "Active Timing Margin Management to Improve Microprocessor Power Efficiency," Electrical and Computer Engineering, The University of Texas at Austin, September 22, 2017.
37. Reena Panda, "Improved Methodology for Evaluating Emerging Applications and Architectures," Electrical and Computer Engineering, The University of Texas at Austin, May 12, 2017.
36. Seogoo Lee, "Approximate High-Level Synthesis of Quality and Energy Optimized Hardware Processors," Electrical and Computer Engineering, The University of Texas at Austin, May 16, 2016. (supervisor)
35. Hugo A. Andrade Bermeo, "Methodology for Design, Synthesis and Deployment of Dependable Systems," Electrical and Computer Engineering, The University of Texas at Austin, May 10, 2016.
34. Balavinayagam Samynathan, "Generating Secure Accelerators Through High Level Compiler," Electrical and Computer Engineering, The University of Texas at Austin, May 2, 2016.

33. Xinnain Zheng, "Learning-based Analytical Cross-Platform Performance and Power Prediction," Electrical and Computer Engineering, The University of Texas at Austin, April 6, 2016. (co-supervisor)
32. Nagaraja Revanna, "Memristor Based Arithmetic Circuit Design," Electrical and Computer Engineering, The University of Texas at Austin, February 25, 2016.
31. Dongwook Lee, "Learning-Based System-Level Power Modeling," Electrical and Computer Engineering, The University of Texas at Austin, November 16, 2015. (supervisor)
30. Dan Zhang, "Accelerating Amorphous Data Parallel Graph Applications using Hardware-Accelerated Priority Schedulers," Electrical and Computer Engineering, The University of Texas at Austin, September 28, 2015.
29. Xiaoyu Ma "Throughput-Oriented Transactional Architecture for FPGA-Accelerated Irregular Problems," Electrical and Computer Engineering, The University of Texas at Austin, March 17, 2015.
28. Subhendu Roy, "Logic and Clock Network Optimization in Nanometer VLSI Circuits," Electrical and Computer Engineering, The University of Texas at Austin, November 19, 2014.
27. Shahrzad Mirkhani, "Statistical Methods for Rapid System Evaluation under Transient and Permanent Faults," Electrical and Computer Engineering, The University of Texas at Austin, June 13, 2014.
26. Maysam Lavasani, "Generating Network-attached Accelerators: Methodology and Applications," Electrical and Computer Engineering, The University of Texas at Austin, December 13, 2013.
25. Yilin Zhang, "Interconnect Optimizations for Nanometer VLSI Design," Electrical and Computer Engineering, The University of Texas at Austin, November 11, 2013.
24. Jhih-Rong Gao, "Lithography aware physical design for manufacturability," Electrical and Computer Engineering, The University of Texas at Austin, September 26, 2013.
23. Minsoo Rhu, "Performance-Efficient Mechanisms for Managing Irregularity in Throughput Processors," Electrical and Computer Engineering, The University of Texas at Austin, August 19, 2013. (chair)
22. Gene Wu, "Automated Abstract Power and Confidence Model Generation," Electrical and Computer Engineering, The University of Texas at Austin, May 2, 2013.
21. Jin Miao, "Design and Synthesis of Approximate Digital Circuits," Electrical and Computer Engineering, The University of Texas at Austin, May 1, 2013. (co-supervisor)
20. Ameya Chaudhari, "Ensuring Software Security and Processor Reliability using Runtime Processor Execution Monitoring," Electrical and Computer Engineering, The University of Texas at Austin, February 6, 2013.
19. Mahesh Prabhu, "Application of Formal Methods to Post-silicon Test and Debug," Electrical and Computer Engineering, The University of Texas at Austin, December 17, 2012.
18. Nicholas Paine, "High Performance Series Elastic Actuation," Electrical and Computer Engineering, The University of Texas at Austin, December 6, 2012.
17. Muhammad Faisal Iqbal, "Efficient System Level Power Management in Communications Processors," Electrical and Computer Engineering, The University of Texas at Austin, October 15, 2012.
16. Parisa Razaghi, "A Host-Compiled Multi-Core Software Simulation Platform," Electrical and Computer Engineering, The University of Texas at Austin, April 4, 2012. (supervisor)
15. Jungwook Sohn, "Improved Architectures for Floating-Point Fused Arithmetic Units," Electrical and Computer Engineering, The University of Texas at Austin, April 4, 2012.
14. Tauseef Raab, "Techniques to Minimize Circuitry and Improve Efficiency for Defect Tolerance," Electrical and Computer Engineering, The University of Texas at Austin, March 7, 2012.
13. Hari Angepat, "Accelerating Multicore System Design Through Functional Timing Decomposition," Electrical and Computer Engineering, The University of Texas at Austin, October 7, 2011.

12. Dylan Pfeifer, "Heterogeneous, Multi-Domain, Mixed Signal Hardware/Software Co-simulation," Electrical and Computer Engineering, The University of Texas at Austin, June 30, 2011. (co-supervisor)
11. Ku He, "Adaptive Low-Energy Techniques in Memory and Digital Signal Processing Design," Electrical and Computer Engineering, The University of Texas at Austin, April 29, 2011. (co-supervisor)
10. Ardavan Pedram, "Algorithm-Architecture Co-Design of a High Performance, Low Power Linear Algebra Processor," Electrical and Computer Engineering, The University of Texas at Austin, April 27, 2011. (co-supervisor)
9. Evgeni Krimer, "Improving Energy Efficiency of Massively Parallel Architectures," Electrical and Computer Engineering, The University of Texas at Austin, April 15, 2011.
8. Nikhil Patel, "Enforcing Architectural Contracts in High-Level Synthesis," Electrical and Computer Engineering, The University of Texas at Austin, March 7, 2011.
7. Ahmed Abdel Hadi, "Multicast Networks: Capacity, Algorithms and Implementation," Electrical and Computer Engineering, The University of Texas at Austin, August 23, 2010. (co-supervisor)
6. Rudrajit Dutta, "Enhancing Memory ECC through Post-Silicon Optimization," Electrical and Computer Engineering, The University of Texas at Austin, May 13, 2010.
5. Wooyoung Jang, "Architecture and Physical Design for Advanced Networks-on-Chip," Electrical and Computer Engineering, The University of Texas at Austin, December 2, 2009.
4. Shayak Banerjee, "Electrically-Driven Optical Proximity Correction and Applications," Electrical and Computer Engineering, The University of Texas at Austin, May 15, 2009.
3. Mark McDermott, "Cognitive Sensor Platform," Electrical and Computer Engineering, The University of Texas at Austin, May 1, 2009.
2. Sriram Sambamurthy, "Power Estimation of Microprocessors", Electrical and Computer Engineering, The University of Texas at Austin, December 1, 2008.
1. Pramod Chandraiah, "Source Re-Coder for SoC Specification Development," Electrical Engineering and Computer Science, University of California, Irvine, September 6, 2005.

M.S. Thesis Supervised

5. Abhishek Das, "simCUDA: A C++ based CUDA Simulation Framework," Electrical and Computer Engineering, The University of Texas at Austin, May 2016.
4. Darshan Dhimantkumar Gandhi, "Core Level Thermal Estimation Techniques for Early Design Space Exploration," Electrical and Computer Engineering, The University of Texas at Austin, May 2014. (co-supervisor with Prof. L. K. John)
3. Jin Miao, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," Electrical and Computer Engineering, The University of Texas at Austin, December 2012. (co-supervisor with Prof. M. Orshansky)
2. Ashmita Sinha, "Multi-Objective Trade-Off Exploration For Cyclo-Static And Synchronous Dataflow Graphs," Electrical and Computer Engineering, The University of Texas at Austin, August 2012.
1. Arindam Goswami, "ExtractCFG: A Framework to Enable Accurate Timing Back Annotation of C Language Source Code," Electrical and Computer Engineering, The University of Texas at Austin, August 2011.

M.S. Reports Supervised

7. Malek Srour, "Data-Dependent Cycle-Accurate Power Modeling of RTL-Level IPs Using Machine Learning," Electrical and Computer Engineering, The University of Texas at Austin, May 2018.
6. Wenxiao Yu, "MASES: Mobility And Slack Enhanced Scheduler For Synchronous Dataflow Graphs," Electrical and Computer Engineering, The University of Texas at Austin, May 2015.

5. Manan Kathuria, "A Framework for Automation of System-level Design Space Exploration," Electrical and Computer Engineering, The University of Texas at Austin, May 2012.
4. John Patrick Tourish, "dspIP: A TCP/IP Implementation for a Digital Signal Processor," Master of Science in Engineering, The University of Texas at Austin, May 2011.
3. Pablo Salinas Bomfim, "Integration of Virtual Platform Models into a System-Level Design Framework," Electrical and Computer Engineering, The University of Texas at Austin, May 2010.
2. Joel Williams, "Prototyping of MP3 Decoding and Playback on an ARM-based FPGA Development Board," Master of Science in Engineering, The University of Texas at Austin, May 2010.
1. Peter James Overholt, "Desktop Simulation of a Digital Signal Processing Design Flow using Synchronous Dataflow Modeling," Master of Science in Engineering, The University of Texas at Austin, August 2009.

M.S. Thesis Committee Member

9. Yuxin Wang, "Extending Capability of Formal Tools: Applying Semiformal Verification on Large Design," Electrical and Computer Engineering, The University of Texas at Austin, May 2019.
8. Daniel Ruiz Santa Maria, "Identifying Post-Silicon Bugs and Their Root Causes Through a Hardware Introspection Engine," Electrical and Computer Engineering, The University of Texas at Austin, August 2017.
7. Sreenivaas Muthyala Sudhakar, "Improving Encoding Efficiency in Test Compression using Sequential Linear Decompressors with Retained Free Variables," Electrical and Computer Engineering, The University of Texas at Austin, May 2013.
6. Donald E. Owen Jr., "The Feasibility of Memory Encryption and Authentication," Electrical and Computer Engineering, The University of Texas at Austin, April 2013.
5. Gaurav Nolkha, "Scaling and Improving Mapping of Module Level Vectors to Software Based Self Tests," Electrical and Computer Engineering, The University of Texas at Austin, May 2009.
4. Eric James Johnson, "Efficient Debugging and Tracing of System Level Designs," Electrical and Computer Engineering, University of California, Irvine, March 2006.
3. Alexander Gluhak, "Development of a Graphical User Interface for a System-On-Chip Design Environment" (in German), Electrical Engineering and Information Technology, University of Applied Sciences, Offenburg, Germany, April 2002.
2. David Berner, "Development of a Visual Refinement and Exploration Tool for SpecC," Electrical Engineering and Information Technology, University of Applied Sciences, Offenburg, Germany, March 2001.
1. Martin von Weymarn, "Development of a Specification Model of the EFR Vocoder," Institute of Computer and Communication Network Engineering, Technical University of Braunschweig, Germany, July 2001.

M.S. Report Committee Member

3. Matthew C. Slowik, "A Flexible Display System for Embedded Applications," Master of Science in Engineering, The University of Texas at Austin, April 2013.
2. Hans L. Yaeger, "Microprocessor Power Management and a Stand-alone Benchmarking Application for Android Based Platforms," Master of Science in Engineering, The University of Texas at Austin, December 2011.
1. Thomas G. Madaelil, "Clock Gating for Floating Point Units," Master of Science in Engineering, The University of Texas at Austin, December 2009.

Senior Design Projects Mentored

9. R. Butani, A. El-Azizi, D. Gipson, P. Rama, D. Rollins, J. Yang, J. Zhang, "Undergraduate Teaching Platform," Electrical and Computer Engineering, The University of Texas at Austin, September 2019-May 2020. (Honors Project) (co-supervised with M. Erez)

8. N. Dao, J. Eustaquio, V. Tran, C. Ascensio, I. Villamiel, J. Luebbe, A. Stahl "Deep Learning Hardware Accelerator," Electrical and Computer Engineering, The University of Texas at Austin, September 2019-May 2020. (Honors Project)
7. Alex Dexter, Robert Streit, Brian Wang, Leigh Gonik, Shyam Sabhaya, Zachary Susskind, "Deep Learning Hardware Accelerator," Electrical and Computer Engineering, The University of Texas at Austin, September 2018-May 2019. (Honors Project)
6. Karan Gujral, Zohaib Imam, Justin Liang, Dung Nguyen, Nick White, Kevin Wong, "Occupied: An Internet of Things Network," Electrical and Computer Engineering, The University of Texas at Austin, September 2017-May 2018.
5. Nick Corti, Sean Gajjar, Charlie Gao, James Morris, Daniel Zelada, "HomeSight," Electrical and Computer Engineering, The University of Texas at Austin, January-May 2016. (Entrepreneur project)
4. Saad Ahmed, Aleyas Kulmadayil, Manav Mandhani, Eric Maras, Jeremy Martin, Zhambyl Shaikhonov, Bharatendu Soumil, "Xilinx Smart Home Hub," Electrical and Computer Engineering, The University of Texas at Austin, January-December 2015.
3. Juan Cano, Dean Daskalantonakis, John Johnson, Zander Smith, Kartik Tiwari, Kate Walker, "DrillSim9000," Electrical and Computer Engineering, The University of Texas at Austin, January-December 2014.
2. Kevin Johns, Andy Kaplan, Martin Lin, Ali Mohandesi, Justin Prukop, "Digital Post-It Note," Electrical and Computer Engineering, The University of Texas at Austin, August 2012-May 2013.
1. Victor Azurin, Robert Graham, Maykel Hanna, Mina Hanna, Shantu Jain, "MRI Simulation," Electrical and Computer Engineering, The University of Texas at Austin, August 2011-May 2012.

Visiting Researchers Co-Advised

1. Slim Ben Saoud, Fullbright Fellow, Electrical and Computer Engineering, National Institute of Applied Sciences and Technology, Tunisia, 2002.

PRESENTATIONS

Keynotes, Plenaries and Distinguished Lectures

2. "System-Level and Hardware-Software Co-Design: Past, Present and Future," Special Session on SAMOS XV, *15th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XV)*, Samos, Greece, July 2015.
1. "Software Synthesis for Embedded Multicore Systems," Keynote, *Brazilian Symposium on Computing System Engineering (SBESC)*, Florianopolis, Brazil, November 2011.

Tutorials

9. "Network-Level Design of IoT and Edge Computing Systems," in *Embedded Systems: Invisible Computing*, full-day tutorial with T. Mitra (organizer), L. Carloni and S. Parameswaran, International Conference on VLSI Design and Embedded Systems (VLSID), Bengaluru, India, January 2020.
8. "Designing Multi-Processor and Multi-Core Systems-on-Chip," embedded tutorial, Austin Conference on Integrated Systems and Circuits (ACISC), Austin, Texas, October 2009.
7. "Modeling, Synthesis and Verification," in *System-Level Modeling, Analysis and Synthesis of Embedded Multi-core Designs*, full-day tutorial with S. Abdi, C. Haubelt, W. Ecker, M. Meredith, M. Speitel, J. Teich, D. Gajski (organizer), Design, Automation and Test in Europe (DATE) Conference, Nice, France, April 2009.
6. "Principles of Embedded Systems: Modeling, Synthesis and Verification," in *High-Level Design*, two-day tutorial with M. Fujita (organizer), D. Gajski, S. Abdi, VLSI Design Education Center (VDEC), Tokyo, Japan, January 2008.

5. "Embedded System Modeling," in *Concepts and Tools for Practical Embedded System Design*, half-day tutorial with S. Abdi, D. Gajski, N. Dutt (organizer), IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, January 2007.
4. "System-Level Modeling and Design: Experimentation with SpecC," in *System Level Specification beyond RTL*, half-day tutorial with J. Zhu, A. Jerraya, D. Gajski (organizer), Design, Automation and Test in Europe (DATE) Conference, Paris, France, March 2002.
3. "Modeling and Design with SpecC" and "Design of a GSM Vocoder," in *SpecC Language and Design Methodology*, half-day tutorial with T. Ishii, J. Zhu, D. Gajski (organizer), Design, Automation and Test in Europe (DATE) Conference, Munich, Germany, March 2001.
2. "Modeling and Design with SpecC" and "Design of a GSM Vocoder," in *SpecC Language and Design Methodology*, two-day tutorial with R. Dömer, D. Gajski, Motorola Semiconductor Products Section, Austin, April 2001.
1. "Modeling and Design with SpecC," in *SpecC Language and Design Methodology*, full-day tutorial with T. Ishii, J. Zhu, M. Olivarez, C. Siska, D. Araki, D. Gajski (organizer), IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, January 2001.

Invited Conference and Workshop Presentations

10. "Learning-Based Hardware/Software Performance and Power Modeling," *ACM/IEEE Workshop on Machine Learning for CAD*," Canmore, Canada, September 2019.
9. "Predictive Modeling for Heterogeneous System Design," *Workshop on Modeling & Simulation of Systems and Applications (ModSim)*, Seattle, WA, August 2019.
8. "System-Level Design Research," *SiFive RISC-V Tech Symposium*, Austin, TX, February 2019.
7. "Learning-Based HW/SW Performance and Power Prediction," *edaWorkshop*, Dresden, Germany, May 2017.
6. "Modeling and Prototyping of Cyber-Physical Networks-of-Systems," NII Shonan Meeting 073 *Architecture-Centric Modeling, Analysis, and Verification of Cyber-Physical Systems*, National Institute of Informatics (NII), Shonan Village Center (SVC), Japan, March 2016.
5. "Quality-Energy Aware System Design," Dagstuhl Seminar 15491 *Approximate and Probabilistic Computing: Design, Coding, Verification*, Schloss Dagstuhl – Leibniz Zentrum für Informatik, Wadern, Germany, November 2015.
4. "Learning-Based Analytical Power and Performance Modeling," Intel DTS Annual Symposium on VLSI CAD and Validation: *Big Data Analytics for CAD Applications*, Technion, Haifa, Israel, November 2015.
3. "Dataparallel Accelerator Design beyond GPUs," IEEE CTS CAS/SSC/CEDA Workshop on *Data Parallelism for Multi-Core Chips and GPU*, Austin, TX, October 2012.
2. "Teaching Experience: Developing a Class on Embedded Systems," in *Young Faculty Workshop*, ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, June 2012.
1. "OS and Processor Modeling," in workshop on *Hardware Dependent Software (HdS)*, ACM/IEEE Design Automation Conference (DAC), San Diego, June 2007.

Invited Lectures and Talks

74. "Network-Level Design for IoT Edge Computing," Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano, Italy, October 2018.
73. "Learning-Based Hardware/Software Performance and Power Prediction," Max-Planck Institute for Software Systems (MPI-SWS), Kaiserslautern, Germany, June 2018.
72. "Learning-Based Power and Performance Prediction for Heterogeneous System Design," Computer Engineering & Systems Group (CESG) Seminar, Texas A&M University (TAMU), April 2018.
71. "Learning-Based System-Level Power and Performance Prediction," Samsung Austin Technical Forum on "Machine Learning – From Enabling Hardware to Neural Nets to Neural Interpretation," Samsung Austin R&D Center (SARC), October 2017.

70. “Domain-Specific Linear Algebra Compute Fabrics,” Infineon, Munich, Germany, July 2017.
69. “Learning-Based Models for Power- and Performance-Aware System Design,” Chair for Electronic Design Automation, Department of Electrical and Computer Engineering, Technical University of Munich (TUM), Munich, Germany, July 2017.
68. “Learning-Based System-Level Power and Performance Prediction,” Center for Advancing Electronics Design (cfaed), Technical University Dresden, Dresden, Germany, May 2017.
67. “Learning-Based System-Level Power and Performance Prediction,” Institute of Computer Technology, Technical University Wien (TUW), Vienna, Austria, March 2017.
66. “Learning-Based System-Level Power and Performance Prediction,” Infineon, Munich, Germany, February 2017.
65. “Quality-Energy Aware Design of Approximate Computing Systems,” ITG/GMM/GI Fachausschusses RSS-LG ("Leitungsgremium Rechnergestützter Schaltungs- und Systementwurf"), Verband der Elektrotechnik, Elektronik und Informationstechnik (VDE), Frankfurt, Germany, December 2016.
64. “Learning-Based System-Level Power and Performance Prediction,” Department Colloquium, Department of Computer Science, University of Tübingen, Germany, December 2016.
63. “Learning-Based System-Level Power and Performance Prediction,” Systems Group Seminar, Department of Computer Science, ETH Zürich, Switzerland, November 2016.
62. “Performance and Power Modeling of Cyber-Physical Networks-of-Systems,” Corporate Research, Robert Bosch GmbH, Renningen, Germany, October 2016.
61. “Quality-Energy Aware Design of Approximate Computing Systems,” Fujita Laboratory, Department of Electrical Engineering and Information Systems (EEIS), School of Engineering, Tokyo University, Tokyo, Japan, March 2016.
60. “System-Level Design of Energy-Efficient MPSoCs,” ARM/UT Day, The University of Texas at Austin, Austin, TX, October 2015.
59. “Performance & Power Aware SoC Design: Specializations, Approximations & Models,” Qualcomm/UT Day, Qualcomm Corporate R&D, San Diego, CA, June 2015.
58. “Host-Compiled Performance, Energy, Reliability, Power and Thermal (PERPT) Modeling for Fast & Accurate Virtual Platform Prototyping,” Cadence Design Systems, IP Solutions/Tensilica group, San Jose, CA, June 2015.
57. “Energy-Aware Design of Approximate & Heterogeneous Computing Systems,” Qualcomm Silicon Valley Resarch (QSVR), San Jose, CA, June 2015.
56. “Quality-Energy Aware Design of Approximate Computing Systems,” Chair for Embedded Systems, Department of Computer Science, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, December 2014.
55. “Multi-dimensional Modeling, Design and Exploration of Heterogeneous Multicore SoCs,” Freescale, Munich, Germany, December 2014.
54. “Quality-Energy Aware Design of Approximate Computing Systems,” Institute for Integrated Systems/Institute for Electronic Design Automation, Department of Electrical and Computer Engineering, Technical University Munich (TUM), Germany, December 2014.
53. “Energy-Efficient Design of Domain-Specific Compute Fabrics,” Department of Electrical and Computer Engineering, Northeastern University, October 2013.
52. “Energy-Efficient Design of Domain-Specific Compute Fabrics,” Computer Science and Artificial Intelligence Laboratory (CSAIL), Massachusetts Institute of Technology (MIT), October 2013.
51. “Energy-Efficient System Design,” Computer Engineering and Systems Group (CESG) Seminar, Electrical and Computer Engineering, Texas A&M University, College Station, Texas, September 2013.

50. "System-Level Design of Embedded Networks-of-Systems," Samsung Telecommunications America, Dallas, Texas, August 2013.
49. "Energy-Efficient System Design," Huawei Technologies USA, Dallas, Texas, August 2013.
48. "System-Level Design of Embedded Systems," Department of Electrical Engineering and Information Technology, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, June 2013.
47. "Models and Architectures for Heterogeneous System Design," Department of Computer Science, University of California, Los Angeles, Los Angeles, CA, May 2013.
46. "Host-Compiled System Models for Early Power and Performance Exploration," Qualcomm Technologies (QCT), Inc., San Diego, CA, May 2013.
45. "Models and Architectures for Heterogeneous System Design," Department of Computer Science and Engineering, University of California, San Diego, San Diego, CA, May 2013.
44. "Models and Architectures for Heterogeneous System Design," Center for Embedded Computer Systems (CECS), University of California, Irvine, Irvine, CA, May 2013.
43. "Models and Architectures for Heterogeneous System Design," Center for Experimental Research in Computer Systems (CERCS), Georgia Institute of Technology, Atlanta, GA, April 2013.
42. "Models and Architectures for Heterogeneous System Design," Design of Robotics and Embedded Systems, Analysis and Modeling Seminar (DREAMS), Center for Electronic System Design/Center for Hybrid and Embedded Software Systems (CHESS), University of California, Berkeley, Berkeley, CA, April 2013.
41. "Models and Architectures for Heterogeneous System Design," Center for Silicon System Implementation (CSSI), Carnegie Mellon University, Pittsburgh, PA, April 2013.
40. "Heterogeneous System Design," Intel Research, Hillsboro, Oregon, March 2012.
39. "A Low-Power, High-Performance Linear Algebra Core," NSF Center for Embedded Systems, Faculty of Computer Science and Engineering, Arizona State University, February 2012.
38. "A Low-Power, High-Performance Linear Algebra Core," Tech Topics Seminar Series, Advanced Micro Devices (AMD), Austin, TX, November 2011.
37. "Circuit-Level Timing-Error Acceptance for Low Energy Signal Processing," Cirrus Logic, Austin, TX, November 2011.
36. "Using Cutting-Edge Tools for Communication System Design," National Instruments NIWeek conference, Austin, TX, August 2011.
35. "System-Level Design of Heterogeneous Embedded Multi-Core Platforms," Department of Informatics, University of Tübingen, Germany, June 2011.
34. "Low Power, High Performance Linear Algebra Processing," IBM Austin Research Lab, Austin, Texas, May 2011.
33. "System-Level Design of Heterogeneous Embedded Multi-Core Platforms," Huawei Technologies USA, Dallas, Texas, March 2011.
32. "Embedded System Design Challenges and Trends," Texas Instruments, Dallas, Texas, March 2011.
31. "Embedded Systems Research," 3M, Austin, Texas, January 2011.
30. "System-Level Design of Multi-Processor/Multi-Core Systems-on-Chip," Intel Research, Hillsboro, Oregon, November 2010.
29. "System-Level Design for Heterogeneous Low-Power and High-Performance Compute Fabrics," National Instruments, Austin, Texas, October 2010.
28. "Heterogeneous Computing and the System-Level Design Challenge," Advanced Micro Devices (AMD), Austin, Texas, August 2010.
27. "System-Level Design of Embedded Multi-Processor/Multi-Core Systems-on-Chip," National Instruments, Berkeley Research Lab, June 2010.

26. "System-Level Design of Multi-Processor/Multi-Core System-on-Chip," Qualcomm, Bay Area Research and Development (BARD), San Jose, CA, June 2010.
25. "Designing Multi-Processor and Multi-Core Systems-on-Chip," IEEE Central Texas SSC/CAS Chapter, Austin, Texas, February, 2010.
24. "Electronic System Level Modeling for Automated MPSoC Design and Exploration," IBM Research & Development, Böblingen, Germany, August 2009.
23. "High-Level Programming, Prototyping and Synthesis of MPSoC Software," Department of Computer Science, University of Erlangen-Nuremberg, Germany, July 2009.
22. "Electronic System Level Modeling for Automated MPSoC Design and Exploration," Freescale, Austin, TX, January 2009.
21. "High-Level Programming, Prototyping and Synthesis of MPSoC Software," Department of Embedded/Real-Time Systems, University of Ulm, Germany, December 2008.
20. "Electronic System Level Modeling for Automated, C-Based MPSoC Design and Exploration," IBM Austin Research Labs, December 2008.
19. "Electronic System Level Modeling, Design and Synthesis of Embedded Computer Systems," National Instruments, Austin, TX, November 2008.
18. "System-Level Modeling for Embedded System Design Automation," Department of Electrical and Computer Engineering, Florida International University, April 2008.
17. "System-Level Modeling for Embedded System Design Automation," Department of Electrical Engineering, University of Hawaii at Manoa, April 2008.
16. "System-Level Modeling for Embedded System Design Automation," Department of Electrical and Computer Engineering, University of Texas at Austin, March 2008.
15. "System-Level Modeling for Embedded System Design Automation," Department of Computer Science and Engineering, University of Texas at Arlington, March 2008.
14. "Automated, C-Based Design of Multi-Processor Systems-On-Chip", Department of Computer Science, University of Erlangen-Nuremberg, Germany, March 2008.
13. "System-Level Modeling for Embedded System Design Automation," Department of Electrical Engineering and Computer Science, University of Kansas, Lawrence, February 2008.
12. "Programming, Modeling and Synthesis of Multi-Processor System Software," Electronics Design Seminar, Department of Electrical and Computer Engineering, University of California, Santa Barbara, February 2008.
11. "Embedded Processor and RTOS Modeling for Rapid, Early MPSoC Design and Validation," Fujita lab, University of Tokyo, Japan, August 2007.
10. "Embedded Processor and RTOS Modeling for Multi-Processor Design and Validation," Institute of Computer Architecture and Computer Engineering, University of Stuttgart, Germany, June 2007.
9. "Embedded Processor and RTOS Modeling for Multi-Processor Design and Validation," Department for Base Technologies & Services, Infineon Technologies AG, Munich, Germany, June 2007.
8. "Embedded Processor and RTOS Modeling for Rapid, Early MPSoC Design and Validation," Institute for Integrated Systems, Munich University of Technology, Munich, Germany, June 2007.
7. "Modeling of Embedded Processors and Real-Time Operating Systems for Rapid, Early Multi-Processor Systems Design and Validation," C-LAB, University of Paderborn, Germany, June 2007.
6. "A System Design Environment for Automatic Model Generation and Prototyping," Research and Advance Development, Robert Bosch GmbH, Schwieberdingen, Germany, March 2006.
5. "Layer-Based Communication Design for Automatic SoC Platform Generation," Department of Computer Engineering, University of Tübingen, October 2005.
4. "Methodology and Environment for System-Level Design," Xilinx Research Laboratories, San Jose, CA, August 2003.

3. "System-Level Design Language, Methodology and Environment," IBM Research and Development, Böblingen, Germany, March 2003.
2. "System-Level Design Language, Methodology and Environment," BMW, Munich, Germany, January 2003.
1. "Modeling and Design with SpecC," C-LAB, University of Paderborn, Germany, March 2001.

CITATIONS

10. Electronic version of the "Embedded System Design: Modeling, Synthesis and Verification" book was one of the top 25% most downloaded eBooks in the relevant Springer eBook collection in 2012.
9. "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets" paper among the IEEE Embedded System Letters' top-five accessed articles in April, August and November 2012.
8. Teaching material developed for "Embedded System Design and Modeling" class in use at several universities worldwide, including Northeastern University, Iowa State University, Concordia University (Canada), Leiden University (Netherlands), Istanbul Technical University (Turkey), the University of Teheran (Iran), the Federal University of Pernambuco (Brazil), and the Universities of Oldenburg and Stuttgart in Germany.
7. "Embedded System Design: Modeling, Synthesis and Verification," book reviewed in IEEE Design & Test, March/April 2010 issue (by Grant Martin), as "great introduction to embedded-systems design methodologies and tools" that is "heartily recommended."
6. "RTOS Modeling for System-Level Design" paper reprinted in the book *Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE*, Springer, 2008.
5. "RTOS Modeling for System-Level Design" paper reprinted as a significant contribution in the book *Embedded Software for SoC*, Kluwer, 2003.
4. "System Design: A Practical Guide with SpecC" book cited in panel "Embedded Systems Education: How to Teach the Required Skills?", *IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Stockholm, Sweden, September 2004.
3. SpecC language and methodology cited in book *System Design with SystemC* (by T. Grötker, S. Liao, G. Martin, S. Swan), Kluwer, 2002, as major reference and inspiration for the development of SystemC, a leading, industry-standard system-level design language.
2. Japanese edition of "SpecC: Specification Language and Methodology" ranked among the top 10 bestselling technical books in Japan.
1. "SpecC: Specification Language and Methodology" and "System Design: A Practical Guide with SpecC" books with over 700 citations (source: Google Scholar).

PUBLICATIONS (titles are embedded hyperlinks):

Books

B7. D. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, *Embedded System Design: Modeling, Synthesis, Verificatio*n, Springer, ISBN 978-1-4419-0503-1, September 2009.

B6. A. Rettberg, M. Zanella, R. Dömer, A. Gerstlauer, F. Rammig (editors), *Embedded System Design: Topics, Techniques and Trends*, Springer, ISBN 978-0-387-72257-3, June 2007.

B5. A. Gerstlauer, R. Dömer, J. Peng, D. D. Gajski, *System Design: A Practical Guide with SpecC*, Chinese Edition, Translated by Jinian Bian and Hongxi Xue, Tsinghua University Press, China, ISBN 978-7-302-13289-9, January 2008.

B4. A. Gerstlauer, R. Dömer, J. Peng, D. D. Gajski, *System Design: A Practical Guide with SpecC*, Japanese Edition, Translated by Tsuneo Kinoshita, SpecC Technology Open Consortium, Japan, June 2001.

B3. A. Gerstlauer, R. Dömer, J. Peng, D. D. Gajski, *System Design: A Practical Guide with SpecC*, Kluwer Academic Publishers, ISBN 0-7923-7387-1, June 2001.

B2. D. D. Gajski, J. Zhu, R. Dömer, A. Gerstlauer, S. Zhao, Sp*ecC: Specification Language and Methodology*, Japanese Edition, Translated by Tsuneo Kinoshita, CQ Publishing, Japan, ISBN 4-7898-3353-4, December 2000.

B1. D. D. Gajski, J. Zhu, R. Dömer, A. Gerstlauer, S. Zhao, *SpecC: Specification Language and Methodology*, Kluwer Academic Publishers, ISBN 0-7923-7822-9, March 2000.

Book Chapters

P11. S. Lee, A. Gerstlauer, "Approximate High-Level Synthesis of Custom Hardware," in S. Reda, M. Shafique (eds.), *Approximate Circuits: Methodologies and CAD*, Springer, ISBN 978-3-319-99321-8, 2019.

P10. D. Mueller-Gritschneder, A. Gerstlauer, "Host-Compiled Simulation," in S. Ha, J. Teich (eds.), *Handbook of Hardware/Software Co-Design*, Springer, ISBN 978-94-017-7358-4, 2017.

P9. G. Schirner, A. Gerstlauer, R. Dömer, "SCE: System-on-Chip Environment," in S. Ha, J. Teich (eds.), *Handbook of Hardware/Software Co-Design*, Springer, ISBN 978-94-017-7358-4, 2017.

P8. S. Ha, J. Teich, C. Haubelt, M. Glaß, T. Mitra, R. Dömer, P. Eles, A. Shrivastava, A. Gerstlauer, S. S. Bhattacharyya, "Introduction to Hardware/Software Codesign," in S. Ha, J. Teich (eds.), *Handbook of Hardware/Software Co-Design*, Springer, ISBN 978-94-017-7358-4, 2017.

P7. V. Joloboff, A. Gerstlauer, "Virtual Prototyping: An Overview," in S. Nakajima, J.-P. Talpin, M. Toyoshima, H. Yu (eds.), *Cyber-Physical System Design from an Architecture Analysis Viewpoint*, Communications of NII Shonan Meetings, Springer, ISBN 978-981-10-4435-9, 2017.

P6. S. Lee, A. Gerstlauer, "Fine Grain Precision Scaling for Datapath Approximations in Digital Signal Processing Systems," in A. Orailoglu, H. F. Ugurdag, L. M. Silveira, M. Margala, R. Reis (eds.), *VLSI-SoC: At the Crossroads of Emerging Trends*, Revised Selected Papers of the 21st IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2013), Springer, ISBN 978-3-319-23798-5, October 2015.

P5. G. Schirner, R. Dömer, A. Gerstlauer, "High-Level Development, Modeling and Automatic Generation of Hardware-Dependent Software," in W. Ecker, W. Mueller, R. Dömer (eds.), *Hardware-Dependent Software: Principles and Practice*, Springer, ISBN 978-1-4020-9435-4, January 2009.

P4. H. Zabel, W. Mueller, A. Gerstlauer, "Accurate RTOS Modeling and Analysis with SystemC," in W. Ecker, W. Mueller, R. Dömer (eds.), *Hardware-Dependent Software: Principles and Practice*, Springer, ISBN 978-1-4020-9435-4, January 2009.

P3. A. Gerstlauer, H. Yu, D. D. Gajski, "RTOS Modeling for System-Level Design," in R. Lauwereins, J. Madsen (eds.), *Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE*, Springer, ISBN 978-1-4020-6487-6, March 2008.

P2. A. Gerstlauer, H. Yu, D. D. Gajski, "RTOS Modeling for System-Level Design," in A. A. Jerraya, S. Yoo, N. When, D. Verkest (eds.), *Embedded Software for SoC*, Kluwer Academic Publishers, ISBN 1-4020-7528-6, June 2003.

P1. A. Rettberg, F. J. Rammig, A. Gerstlauer, D. D. Gajski, W. Hardt, B. Kleinjohann, "The Specification Language SpecC within the PARADISE Design Environment," in B. Kleinjohann (ed.), *Architecture and Design of Distributed Embedded Systems*, Kluwer Academic Publishers, ISBN 0-7923-7345-6, April 2001.

Journal Papers

J26. P. Stanley-Marbell, A. Alaghi, M. Carbin, E. Darulova, L. Dolecek, A. Gerstlauer, G. Gillani, D. Jevdjic, T. Moreau, M. Cacciotti, A. Daglis, N. Enright Jerger, B. Falsafi, S. Misailovic,

A. Sampson, D. Zufferey, “Exploiting Errors for Efficiency: A Survey from Circuits to Algorithms,” *ACM Computing Surveys*, accepted for publication, arXiv preprint arXiv:1809.05859, January 2020.

J25. K. Mirzazad Barijough, Z. Zhao, A. Gerstlauer, “Quality/Latency-Aware Real-time Scheduling of Distributed Streaming IoT Applications,” ACM Transactions on Embedded Computer Systems (TECS), Special Issue on Embedded Systems Week (ESWEEK) 2019, International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), vol. 18, no. 5s, pp. 83:1-83:23, October 2019. (27% acceptance rate)

J24. H. Amrouch, S. B. Ehsani, A. Gerstlauer, J. Henkel, "On the Efficiency of Voltage Overscaling under Temperature and Aging Effects, *IEEE Transactions on Computers (TC)*, vol. 68, no. 11, pp. 1647-1662, November 2019.

J23. Z. Zhao, K. Mirzazad Barijough, A. Gerstlauer, “DeepThings: Distributed Adaptive Deep Learning Inference on Resource-Constrained IoT Edge Clusters,” *IEEE Transactions on Computer-Aided Design (TCAD)*, Special Issue on Embedded Systems Week (ESWEEK) 2018, International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), vol. 37, no. 11, pp. 2348-2359, October 2018. (26% acceptance rate)

J22. S. Song, X. Liu, Q. Wu, A. Gerstlauer, T. Li, L. K. John, “Start Late or Finish Early: A Distributed Graph Processing System with Redundancy Reduction,” *Proceedings of the VLDB Endowment (PVLDB)*, vol. 12, no. 12, pp. 154-168, October 2018.

J21. S. Lee, A. Gerstlauer, “Data-Dependent Loop Approximations for Performance-Quality Driven High-Level Synthesis,” *IEEE Embedded System Letters (ESL)*, vol. 10, no. 1, pp. 18-12, March 2018.

J20. D. Lee, A. Gerstlauer, “Learning-Based, Fine-Grain Power Modeling of System-Level Hardware IPs,” *ACM Transactions on Design Automation for Electronic Systems (TODAES)*, vol. 23, no. 3, pp. 30:1-30:25, February 2018.

J19. S. Francis, A. Gerstlauer, “A Reactive and Adaptive Data Flow Model For Network-of-System Specification,” *IEEE Embedded System Letters (ESL)*, vol. 9, no. 4, pp. 121-124, December 2017.

J18. X. Zheng, L. K. John, A. Gerstlauer, “LACross: Learning-Based Analytical Cross-Platform Performance and Power Prediction,” *International Journal of Parallel programming (IJPP)*, Special Issue on SAMOS XV, vol. 45, no. 6, pp. 1488-1514, December 2017.

J17. Z. Zhao, A. Gerstlauer, L. K. John, “Source-Level Performance, Energy, Reliability, Power and Thermal (PERPT) Simulation,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 2, pp. 299-312, February 2017.

J16. P. Razaghi, A. Gerstlauer, “Host-Compiled Multi-Core System Simulation for Early Real-Time Performance Evaluation,” *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 13, no. 5s, pp. 166:1-166:26, November 2014.

J15. A. Pedram, J. D. McCalpin, A. Gerstlauer, “A Highly Efficient Multicore Floating-Point FFT Architecture Based on Hybrid Linear Algebra/FFT Cores,” *Journal of Signal Processing Systems*, Special Issue on Application Specific Processors and Architectures, vol. 77, no. 1-2, pp. 169-190, October 2014.

J14. S. Lee, A. Gerstlauer, R. W. Heath, “Distributed Real-time Implementation of Interference Alignment with Analog Feedback,” *IEEE Transactions on Vehicular Technology (TVT)*, vol. 64, no. 8, pp. 3513-3525, September 2014.

J13. A. Pedram, A. Gerstlauer, R. A. van de Geijn, “Algorithm, Architecture, and Floating-Point Unit Codesign of a Matrix Factorization Accelerator,” *IEEE Transactions on Computers (TC)*, Special Section on Computer Arithmetic, vol. 63, no. 8, pp. 1854-1867, August 2014.

J12. D. Pfeifer, J. Valvano, A. Gerstlauer, “SimConnect and SimTalk for Distributed Cyber-Physical System Simulation,” *Simulation: Transactions of the Society for Modeling and Simulation International*, vol. 89, no. 10, pp. 1254-1271, October 2013.

J11. K. He, A. Gerstlauer, M. Orshansky, "Circuit-Level Timing-Error Acceptance for Design of Energy-Efficient DCT/IDCT-based Systems," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 3, no. 6, pp. 961-974, June 2013.

J10. J. Lin, A. Gerstlauer, B. L. Evans, "Communication-Aware Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Journal of Signal Processing Systems*, vol. 69, no. 3, pp. 279-291, December 2012.

J9. A. Pedram, R. A. van de Geijn, A. Gerstlauer, "Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," *IEEE Transactions on Computers (TC)*, Special Issue on Energy Efficient Computing, vol. 61, no. 12, pp. 1724-1736, December 2012. (18% acceptance rate)

J8. P. Razaghi, A. Gerstlauer, "Predictive OS Modeling for Host-Compiled Simulation of Periodic Real-Time Task Sets," *IEEE Embedded System Letters*, vol. 4, no. 1, pp. 5-8, March 2012.

J7. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, J. Teich, "Automatic System-Level Synthesis: From Formal Application Models to Generic Bus-Based MPSoCs," *Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC)*, vol. 5, no. 4, 2011.

J6. G. Schirner, A. Gerstlauer, R. Dömer, "Fast and Accurate Processor Models for Efficient MPSoC Design," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 15, no. 2, article no. 10, pp. 1-26, February 2010.

J5. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski, J. Teich, "Electronic System-Level Synthesis Methodologies," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 10, pp. 1517-1530, October 2009.

J4. R. Dömer, A. Gerstlauer, J. Peng, D. Shin, L. Cai, H. Yu, S. Abdi, D. D. Gajski, "System-on-Chip Environment: A SpecC-based Framework for Heterogeneous MPSoC Design," *EURASIP Journal on Embedded Systems (JES)*, vol. 2008, Article ID 647953, 13 pages, 2008.

J3. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "An Interactive Design Environment for C-Based High-level Synthesis of RTL Processors," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 16, no. 4, pp. 466-475, April 2008.

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J1. S. B. Saoud, A. Gerstlauer, D. D. Gajski, "Codesign Methodology of Real-Time Embedded Controllers for Electromechanical Systems," *American Journal of Applied Sciences*, vol. 2, no. 9, pp. 1331-1336, October 2005.

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C95. M. Asri, C. Dunham, R. Rusitoru, A. Gerstlauer, J. Beard, "The Non-Uniform Compute Device (NUCD) Architecture for Lightweight Accelerator Offload," *Proceedings of the Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP)*, Västerås, Sweden, March 2020.

C94. K. Punniyamurthy, A. Gerstlauer, "Off-Chip Congestion Management for GPU-based Non-Uniform Processing-in-Memory Networks," *Proceedings of the Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP)*, Västerås, Sweden, March 2020.

C93. K. Punniyamurthy, S. Das, A. Gerstlauer, "Cacheline Utilization-Aware Link Traffic Compression for Modular GPUs," *Proceedings of the International Conference on VLSI Design and the International Conference on Embedded Systems (VLSID)*, Bengaluru, India, January 2020. (12% acceptance rate)

C92. A. K. Ananda Kumar, A. Gerstlauer, "Learning-Based CPU Power Modeling," *Proceedings of the ACM/IEEE Workshop on Machine Learning for CAD*, Canmore, Canada, September 2019.

C91. R. Stahl, Z. Zhao, D. Mueller-Gritschneder, A. Gerstlauer, U. Schlichtmann, "Fully Distributed Deep Learning Inference on Resource-Constrained Edge Devices," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, July 2019.

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C89. S. Wei, A. Aysu, M. Orshansky, A. Gerstlauer, M. Tiwari, "Using Power-Anomalies to Detect Evasive Micro-Architectural Attacks in Embedded Systems," *Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, Washington, DC, May 2019. (28% acceptance rate) **(best paper candidate)**

C88. J. Whitehouse, Q. Wu, S. Song, E. John, A. Gerstlauer, L. K. John, "A Study of Core Utilization and Residency in Heterogeneous Smart Phone Architectures," *Proceedings of the ACM/SPEC International Conference on Performance Engineering (ICPE)*, Mumbai, India, April 2019.

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C81. W. Lee, R. Panda, D. Sunwoo, J. Joao, A. Gerstlauer, L. K. John, "BUQS: Battery- and User-aware QoS Scaling for Interactive Mobile Devices," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, South Korea, January 2018. (31% acceptance rate)

C80. Z. Zhao, V. Tsoutsouras, D. Soudris, A. Gerstlauer, "Network/System Co-Simulation for Design Space Exploration of IoT Applications," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, July 2017.

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C77. W. Lee, D. Sunwoo, A. Gerstlauer, L. K. John, "Cloud-guided QoS and Energy Management for Mobile Interactive Web Applications," *Proceedings of the IEEE/ACM International Conference on Mobile Software Engineering and Systems (MOBILESoft)*, Buenos Aires, Argentina, May 2017. (short paper, 51% acceptance rate, 23% regular papers, 66% incl. poster papers)

C76. S. Song, R. Desikan, M. Barakat, S. Sundaram, A. Gerstlauer, L. K. John, "Fine-Grain Program Snippets Generator for Mobile Core Design," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Banff, Alberta, Canada, May 2017. (24% acceptance rate, 37% incl. poster papers)

C75. W. Lee, D. Sunwoo, C. D. Emmons, A. Gerstlauer, L. John, "Exploring Heterogeneous-ISA Core Architectures for High-Performance and Energy-Efficient Mobile SoCs," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Banff, Alberta, Canada, May 2017. (poster paper) (24% acceptance rate, 37% incl. poster papers)

C74. X. Zheng, S. Song, H. Vikalo L. K. John, A. Gerstlauer, "Sampling-Based Binary-Level Cross-Platform Performance Estimation," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Lausanne, Switzerland, March 2017. (24% acceptance rate) **(best paper candidate)**

C73. K. Punniyamurthy, B. Boroujerdian, A. Gerstlauer, "GATSim: Abstract Timing Simulation of GPUs," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Lausanne, Switzerland, March 2017. (24% acceptance rate)

C72. S. Lee, L. K. John, A. Gerstlauer, "High-Level Synthesis of Approximate Hardware under Joint Precision and Voltage Scaling," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Lausanne, Switzerland, March 2017. (24% acceptance rate)

C71. S. Song, X. Zheng, A. Gerstlauer, L. K. John, "Fine-grained Power Analysis of Emerging Graph Processing Workloads for Cloud Operations Management," *Proceedings of the IEEE International Conference on Big Data (BigData): Workshop on Big Data for Cloud Operations Management (BDCOM)*, Washington, DC, December 2016.

C70. D. Pfeifer, A. Gerstlauer, J. Valvano, "Adaptive Resolution control in Distributed Cyber-Physical System Simulation," *Proceedings of the ASA/ASIM/ACM/IEEE/IIE/INFORMS/NIST/SCS Winter Simulation conference (WSC)*, Arlington, Virginia, December 2016.

C69. S. Song, M. Li, X. Zheng, M. LeBeane, J. H. Ryoo, R. Panda, A. Gerstlauer, L. K. John, "Proxy-Guided Load Balancing of Graph Processing Workloads on Heterogeneous Clusters," *Proceedings of the IACC International Conference on Parallel Processing (ICPP)*, Philadelphia, PA, August 2016. (21.5% acceptance rate)

C68. J. Wang, A. Khawaja, G. Biros, A. Gerstlauer, L. K. John, "Optimizing GPGPU Kernel Summation for Performance and Energy Efficiency," *Proceedings of the IACC International Conference on Parallel Processing Workshops (ICPPW): International Workshop on Heterogeneous and Unconventional Cluster Architectures and Applications (HUCAA)*, Philadelphia, PA, August 2016.

C67. M. Asri, A. Pedram, L. K. John, A. Gerstlauer, "Simulator Calibration for Accelerator-Rich Architecture Studies," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, July 2016.

C66. R. Panda, X. Zheng, S. Song, J.H. Ryoo, M. LeBeane, A. Gerstlauer, L. K. John, "Genesys: Automatically Generating Representative Training-Sets for Predictive Benchmarking," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, July 2016.

C65. H. Amrouch, B. Khaleghi, A. Gerstlauer, J. Henkel, "Reliability-Aware Design to Suppress Aging," *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 2016. (23% acceptance rate)

C64. X. Zheng, L. K. John, A. Gerstlauer, "Accurate Phase-Level Cross-Platform Power and Performance Estimation," *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 2016. (23% acceptance rate) **(best paper award)**

C63. S. Lee, D. Lee, K. Han, E. Shriver, L. John, A. Gerstlauer, "Statistical Quality Modeling of Approximate Hardware," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, March 2016. (36% acceptance rate)

C62. D. Lee, T. Kim, K. Han, Y. Hoskote, L. K. John, A. Gerstlauer, "Learning-Based Power Modeling of System-Level Black-Box IPs," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2015. (25% acceptance rate)

C61. W. Lee, Y. Kim, J. H. Ryoo, D. Sunwoo, A. Gerstlauer, L. K. John, "PowerTrain: A Learning-based Calibration of McPAT Power Models," *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Rome, Italy, July 2015. (20% acceptance rate, 30% incl. poster presentations)

C60. X. Zheng, P. Ravikumar, L. K. John, A. Gerstlauer, "Learning-based Analytical Cross-Platform Performance Prediction," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, July 2015. **(best paper award)**

C59. D. Lee, L. K. John, A. Gerstlauer, "Dynamic Power and Performance Back-Annotation for Fast and Accurate Functional Hardware Simulation," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, March 2015. (22% acceptance rate)

C58. O. Bringmann, W. Ecker, A. Gerstlauer, A. Goyal, D. Mueller-Gritschneder, P. Sasidharan, S. Singh, "The Next Generation of Virtual Prototyping: Ultra-fast Yet Accurate Simulation of HW/SW Systems," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, March 2015. (invited paper)

C57. A. Khawaja, J. Wang, D. Malhotra, A. Gerstlauer, G. Biros, L. John, "Performance Analysis of HPC Applications with Irregular Tree Data Structures," *Proceedings of the IEEE International Conference on Parallel and Distributed Systems (ICPADS)*, Hsinchu, Taiwan, December 2014. (30% acceptance rate)

C56. J. Miao, A. Gerstlauer, M. Orshansky, "Multi-Level Approximate Logic Synthesis under General Error Constraints," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2014. (25% acceptance rate)

C55. D. Gandhi, A. Gerstlauer, L. John, "FastSpot: Host-Compiled Thermal Estimation for Early Design Space Exploration," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, March 2014.

C54. J. Miao, A. Gerstlauer, M. Orshansky, "Approximate Logic Synthesis under General Error Magnitude and Frequency Constraints," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2013. (26% acceptance rate)

C53. S. Lee, A. Gerstlauer, "Fine Grain Word Length Optimization for Dynamic Precision Scaling in DSP Systems," *Proceedings of the IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Istanbul, Turkey, November 2013. (20% acceptance rate, 28% incl. short papers) **(best paper candidate)**

C52. S. Chakravarty, Z. Zhao, A. Gerstlauer, "Automated, Retargetable Back-Annotation for Host Compiled Performance and Power Modeling," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Montreal, Canada, October 2013. (28% acceptance rate)

C51. A. Mariano, D. Lee, A. Gerstlauer, D. Chiou, "Hardware and Software Implementations of Prim's Algorithm for Efficient Minimum Spanning Tree Computation," in *Embedded Systems: Design, Analysis and Verification*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Paderborn, Germany, edited by G. Schirner, M. Götz, A. Rettberg, M. C. Zanella, F. J. Rammig, vol. 403 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-3-642-38852-1, June 2013.

C50. H. Park, A. Gerstlauer, "Toward a Fast Stochastic Simulation Processor for Biochemical Reaction Networks," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Washington, DC, June 2013. (22% acceptance rate, 36% incl. short papers)

C49. A. Pedram, J. McCalpin, A. Gerstlauer, "Transforming A Linear Algebra Core to An FFT Accelerator," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Washington, DC, June 2013. (22% acceptance rate, 36% incl. short papers)

C48. P. Razaghi, A. Gerstlauer, "Multi-Core Cache Hierarchy Modeling for Host-Compiled Performance Simulation," *Proceedings of the Electronic System Level Synthesis Conference (ESLSyn)*, Austin, TX, June 2013. (38% acceptance rate)

C47. D. Pfeifer, A. Gerstlauer, J. Valvano, "Dynamic Resolution in Distributed Cyber-Physical System Simulation," *Proceedings of the ACM SIGSIM Conference on Principles of Advanced Discrete Simulation (PADS)*, Montreal, Canada, May 2013. (39% acceptance rate)

C46. A. Pedram, A. Gerstlauer, R. A. van de Geijn, "Floating Point Architecture Extensions for Optimized Matrix Factorization," *Proceedings of the 21st IEEE International Symposium on Computer Arithmetic (ARITH21)*, Austin, TX, April 2013. (28% acceptance rate)

C45. K. He, A. Gerstlauer, M. Orshansky, "Low-Energy Digital Filter Design Based on Controlled Timing Error Acceptance," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 2013.

C44. J. Miao, K. He, A. Gerstlauer, M. Orshansky, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, November 2012. (24% acceptance rate)

C43. J. W. Massey, J. Starr, S. Lee, D. Lee, A. Gerstlauer, R. W. Heath, "Implementation of a Real-Time Wireless Interference Alignment Network," *Proceedings of the Asilomar Conference on Signals, Systems and Computers (ACSSC)*, Pacific Grove, CA, November 2012. (invited paper)

C42. D. Lee, H. Park, A. Gerstlauer, "Synthesis of Optimized Hardware Transactors from Abstract Communication Specifications," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Tampere, Finland, October 2012. (28% acceptance rate)

C41. A. Pedram, A. Gerstlauer, R. A. van de Geijn, "On the Efficiency of Register File versus Broadcast Interconnect for Collective Communications in Data-Parallel Hardware Accelerators," *Proceedings of the IEEE International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, New York, NY, October 2012. (28% acceptance rate)

C40. A. Pedram, S. Z. Gilani, N. S. Kim, R. van de Geijn, M. Schulte, A. Gerstlauer, "A Linear Algebra Core Design for Efficient Level-3 BLAS," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Delft, The Netherlands, July 2012. (poster presentation)

C39. K. He, A. Gerstlauer, M. Orshansky, "Low-Energy Signal Processing using Circuit-Level Timing-Error Acceptance," *Proceedings of the IEEE International Conference on Integrated Circuit Design and Technology (ICICDT)*, Austin, TX, May 2012. (invited paper)

C38. A. Gerstlauer, S. Chakravarty, M. Kathuria, P. Razaghi, "Abstract System-Level Models for Early Performance and Power Exploration," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, January 2012. (invited paper)

C37. P. Razaghi, A. Gerstlauer, "Automatic Timing Granularity Adjustment for Host-Compiled Software Simulation," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Sydney, Australia, January 2012. (34% acceptance rate)

C36. D. Pfeifer, A. Gerstlauer, "Expression-Level Parallelism for Distributed Spice Circuit Simulation," *Proceedings of the IEEE/ACM International Symposium on Distributed and Real Time Applications (DS-RT)*, Manchester, United Kingdom, September 2011.

C35. M. S. Lopez, A. Gerstlauer, A. Avila, S. O. Martinez-Chapa, "A Programmable and Configurable Multi-port System-on-Chip for Stimulating Electrokinetically-Driven Microfluidic Devices," *Proceedings of the International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Boston, MA, September 2011.

C34. A. Abdel-Hadi, J. Michel, A. Gerstlauer, S. Vishwanath, "Real-Time Optimization of Video Transmission in a Network of AAVs," *Proceedings of the IEEE Vehicular Technology Conference (VTC)*, San Francisco, CA, September 2011.

C33. A. Pedram, A. Gerstlauer, R. A. van de Geijn, "A High-Performance, Low-Power Linear Algebra Core," *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP)*, Santa Monica, CA, September 2011. (26% acceptance rate)

C32. J. Lin, A. Srivatsa, A. Gerstlauer, B. L. Evans "Heterogeneous Multiprocessor Mapping for Real-Time Streaming Systems," *Proceedings of the IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Prague, Czech Republic, May 2011.

C31. P. Razaghi, A. Gerstlauer, "Host-Compiled Multicore RTOS Simulator for Embedded Real-Time Software Development," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, March 2011. (27% acceptance rate)

C30. K. He, A. Gerstlauer, M. Orshansky, "Controlled Timing-Error Acceptance for Low Energy IDCT Design," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Grenoble, France, March 2011. (27% acceptance rate)

C29. R. Dömer, W. Chen, X. Han, A. Gerstlauer, "Multi-Core Parallel Simulation of System-Level Description Languages," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, January 2011. (invited paper)

C28. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, J. Teich, "A System-Level Synthesis Approach from Formal Application Models to Generic Bus-Based MPSoCs," *Proceedings of the IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, Samos, Greece, July 2010.

C27. A. Gerstlauer, "Host-Compiled Simulation of Multi-Core Platforms," *Proceedings of the IEEE/IFIP International Symposium on Rapid System Prototyping (RSP)*, Washington, DC, June 2010. (invited paper)

C26. A. Gerstlauer, G. Schirner, "Platform Modeling for Exploration and Synthesis," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, January 2010. (invited paper)

C25. G. Schirner, A. Gerstlauer, R. Dömer, "System-Level Development of Embedded Software," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, January 2010. (invited paper)

C24. A. Pedram, D. Craven, A. Gerstlauer, "Modeling Cache Effects at the Transaction Level," in *Analysis, Architectures and Modeling of Embedded Systems*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Langenargen, Germany, edited by A. Rettberg, M. Zanella, M. Amann, M. Keckeisen, F. Rammig, vol. 310 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-3-642-04283-6, September 2009. (**best paper runner-up**)

C23. A. Banerjee, A. Gerstlauer, "Transaction Level Modeling of Best-Effort Channels for Networked Embedded Devices," in *Analysis, Architectures and Modeling of Embedded Systems*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Langenargen, Germany, edited by A. Rettberg, M. Zanella, M. Amann, M. Keckeisen, F. Rammig, vol. 310 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-3-642-04283-6, September 2009.

C22. R. Dömer, A. Gerstlauer, W. Mueller, "Introduction to Hardware-Dependent Software Design," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, January 2009. (invited paper)

C21. A. Gerstlauer, J. Peng, D. Shin, D. Gajski, A. Nakamura, D. Araki, Y. Nishihara, "Specify-Explore-Refine (SER): From Specification to Implementation," *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, June 2008. (invited paper)

C20. G. Schirner, A. Gerstlauer, R. Dömer, "Automatic Generation of Hardware-Dependent Software for MPSoCs from Abstract System Specifications," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Seoul, South Korea, January 2008. (29% acceptance rate)

C19. G. Schirner, G. Sachdeva, A. Gerstlauer, R. Dömer, "Embedded Software Development in a System-Level Design Flow," in *Embedded System Design: Topics, Techniques and Trends*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Irvine, CA, edited by A. Rettberg, M. Zanella, R. Dömer, A. Gerstlauer, F. Rammig, vol. 231 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-0-387-72257-3, June 2007.

C18. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "An Interactive Design Environment for C-based High-Level Synthesis," in *Embedded System Design: Topics, Techniques and Trends*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Irvine, CA, edited by A. Rettberg, M. Zanella, R. Dömer, A. Gerstlauer, F. Rammig, vol. 231 of IFIP Advances in Information and Communication Technology, Springer, ISBN 978-0-387-72257-3, June 2007.

C17. G. Schirner, A. Gerstlauer, R. Dömer, "Abstract, Multifaceted Modeling of Embedded Processors for System Level Design," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, January 2007. (32% acceptance rate)

C16. R. Dömer, A. Gerstlauer, D. Shin, "Cycle-accurate RTL Modeling with Multi-Cycled and Pipelined Components," *Proceedings of the IEEE International SoC Design Conference (ISOCC)*, Seoul, Korea, October 2006.

C15. D. Shin, A. Gerstlauer, J. Peng, R. Dömer, D. D. Gajski, "Automatic Generation of Transaction-Level Models for Rapid Design Space Exploration," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Seoul, Korea, October 2006. (25% acceptance rate)

C14. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "Automatic Generation of Communication Architectures," in *From Specification to Embedded Systems Application*, Proceedings of the IFIP International Embedded Systems Symposium (IESS), Manaus, Brazil, edited by A. Rettberg, M. C. Zanella, F. Rammig, vol. 184 of IFIP On-Line Library in Computer Science, Springer, ISBN 0-387-27557-6, September 2005.

C13. D. Shin, A. Gerstlauer, R. Dömer, D. D. Gajski, "Automatic Network Generation for System-On-Chip Communication Design," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Jersey City, NJ, September 2005. (25% acceptance rate)

C12. A. Gerstlauer, D. Shin, R. Dömer, D. D. Gajski, "System-Level Communication Modeling for Network-On-Chip Synthesis," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Shanghai, China, January 2005. (27% acceptance rate)

C11. L. Cai, A. Gerstlauer, D. Gajski, "Multi-Metric and Multi-Entity Characterization of Applications for Early System Design Exploration," *Proceedings of the IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Shanghai, China, January 2005. (Poster, 40% acceptance rate)

C10. L. Cai, A. Gerstlauer, D. Gajski, "Retargetable Profiling for Rapid, Early System-Level Design Space Exploration," *Proceedings of the ACM/IEEE Design Automation Conference (DAC)*, San Diego, CA, June 2004. (20% acceptance rate)

C9. H. Yu, A. Gerstlauer, D. Gajski, "RTOS Scheduling in Transaction Level Models," *Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis (CODES+ISSS)*, Newport Beach, CA, October 2003. (21% acceptance rate)

C8. A. Gerstlauer, H. Yu, D. D. Gajski, "RTOS Modeling for System-Level Design," *Proceedings of the Design, Automation and Test in Europe (DATE) Conference*, Munich, Germany, March 2003. (17% acceptance rate) **Reprinted as [P3] in *The Most Influential Papers of 10 Years DATE*.**

C7. W. Mueller, R. Dömer, A. Gerstlauer, "The Formal Execution Semantics of SpecC," *Proceedings of the International Symposium on System Synthesis (ISSS)*, Kyoto, Japan, October 2002. (33% acceptance rate)

C6. A. Gerstlauer, D. Gajski, "System-Level Abstraction Semantics," *Proceedings of the International Symposium on System Synthesis (ISSS)*, Kyoto, Japan, October 2002. (33% acceptance rate)

C5. S. B. Saoud, D. Gajski, A. Gerstlauer, "Seamless Approach for the Design of Control Systems for Power Electronics and Electric Drives," *Proceedings of the IEEE International Conference on Systems, Man and Cybernetics (SMC)*, Hammamet, Tunisia, October 2002.

C4. S. B. Saoud, D. D. Gajski, A. Gerstlauer, "Co-dDesign of Embedded Controllers for Power Electronics and Electric Systems," *Proceedings of the IEEE International Symposium on Intelligent Control (ISIC)*, Vancouver, Canada, October 2002.

C3. S. B. Saoud, D. D. Gajski, A. Gerstlauer, "Co-Design of Emulators for Power Electric Processes Using SpecC Methodology," *Proceedings of the 28th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Sevilla, Spain, November 2002.

C2. A. Gerstlauer, S. Zhao, D. Gajski, A. Horak, "SpecC System-Level Design Methodology Applied to the Design of a GSM Vocoder," *Proceedings of the Ninth Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI)*, Kyoto, Japan, April 2000.

C1. M. Bühler, A. Gerstlauer, B. Stöhr, U. G. Baitinger, "Eine geeignete Schaltkreistechnologie für einen 3D-SOI-Prozess mit T-Gate Transistoren" (in German), *8. ITG Fachtagung Mikroelektronik für die Informationstechnik*, Hannover, Germany, March 1998.

Workshop Papers

W14. K. Punniyamurthy, A. Gerstlauer, "Exploring Non-Uniform Processing In-Memory Architectures," *Workshop on Hardware/Software Techniques for Minimizing Data Movement (Min-Move)*, Portland, OR, September 2017.

W13. S. Lee, L. K. John, A. Gerstlauer, "Data Dependent Loop Approximation Technique in High-Level Synthesis," *Workshop on Approximate Computing (AC)*, Pittsburgh, PA, October 2016.

W12. X. Zheng, L. K. John, A. Gerstlauer, "Accurate Phase-Level Cross-Platform Power and Performance Estimation," *SRC TECHCON*, Austin, TX, September 2016. **(best in session award)**

W11. S. Lee, B. Boroujerdian, L. K. John, A. Gerstlauer, "Synthesis of Quality Configurable Systems," *Workshop on Approximate Computing Across the Stack (WAX)*, Atlanta, GA, April 2016.

W10. X. Zheng, L. K. John, A. Gerstlauer, "Learning-based Analytical Cross-Platform Performance Prediction," *SRC TECHCON*, Austin, TX, September 2015.

W9. S. Lee, D. Lee, L. K. John, A. Gerstlauer, "Operation-Level Approximations for Quality-Energy Optimization in Hardware/Software Compilation," Work-in-Progress (WIP) session, *ACM/EDAC/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 2015.

W8. Z. Zhao, D. Lee, A. Gerstlauer, L. K. John, "Host-Compiled Reliability Modeling for Fast Estimation of Architectural Vulnerabilities," *11th IEEE Workshop on Silicon Errors in Logic – System Effects (SELSE)*, Austin, TX, March 2015.

W7. Z. Zhao, G. Morrison, A. Gerstlauer, "Automatic Calibration of Micro-Architecture Description Models," SRC TECHCON, Austin, TX, September 2014.

W6. Z. Zhao, S. Chakravarty, A. Gerstlauer, "Automated, Retargetable Back-Annotation for Host Compiled Performance and Power Modeling," *SRC TECHCON*, Austin, TX, September 2013. **(best in session award)**

W5. J. Miao, A. Gerstlauer, M. Orshansky, "Modeling and Synthesis of Quality-Energy Optimal Approximate Adders," Work-in-Progress (WIP) session, *ACM/EDAC/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 2012.

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W2. R. Dömer, A. Gerstlauer, D. Gajski, "SpecC Methodology for High-Level Modeling," *9th IEEE/DATC Electronic Design Processes Workshop*, Monterey, CA, April 2002.

W1. R. Dömer, A. Gerstlauer, P. Kritzinger, M. Olivarez, "The SpecC System-Level Design Language and Methodology, Part 2", *Embedded Systems Conference (ESC)*, San Francisco, CA, March 2002.

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D2. R. Dömer, A. Gerstlauer, D. Gajski, "SpecC Language Reference Manual, Version 2.0," SpecC Technology Open Consortium (STOC), December 2002.

D1. R. Dömer, A. Gerstlauer, D. Gajski, "SpecC Language Reference Manual, Version 1.0," SpecC Technology Open Consortium (STOC), March 2001.

Patents

T2. L. K. John, R. Panda, X. Zheng, A. Gerstlauer "Generating Sets of Training Programs for Machine Learning Models," US Patent Application 62365522, filed July 2016.

T1. L. K. John, S. Song, A. Gerstlauer "Guided Load Balancing of Graph Processing Workloads on Heterogeneous Clusters," US Patent 10,437,648, filed July 2016, issued October 2019.

Technical Reports

R42. A. Das, A. Gerstlauer "simCUDA: A C++ based CUDA Simulation Framework," CERC, UT Austin, Technical Report UT-CERC-16-01, May 2016.

R41. W. Yu, A. Gerstlauer "MASES: Mobility And Slack Enhanced Scheduler For Synchronous Dataflow Graphs," CERC, UT Austin, Technical Report UT-CERC-15-01, May 2015.

R40. W.-C. Su, P. Razaghi, A. Sinha, A. Gerstlauer, "Design of Flexible Audio Processing Platforms using the System-on-Chip Environment," CERC, UT Austin, Technical Report UT-CERC-12-06, August 2012.

R39. M. Kathuria, A. Gerstlauer, "A Framework for Automation of System-Level Design Space Exploration," CERC, UT Austin, Technical Report UT-CERC-12-05, June 2012.

R38. A. Pedram, A. Gerstlauer, R. van de Geijn, "Co-Design Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures," CERC, UT Austin, Technical Report UT-CERC-12-02, October 2011.

R37. A. Goswami, A. Gerstlauer, "ExtractCFG: A Framework to Enable Accurate Timing Back Annotation of C Language Source Code," CERC, UT Austin, Technical Report UT-CERC-11-02, August 2011.

R36. H. Park, X. Shen, H. Vikalo, A. Gerstlauer, "Algorithm/Architecture Co-Design of a Stochastic Simulation System-on-Chip," CERC, UT Austin, Technical Report UT-CERC-11-01, January 2011.

R35. A. Pedram, A. Gerstlauer, R. van de Geijn, "Towards a High-Performance, Low-Power Linear Algebra Processor," CERC, UT Austin, Technical Report UT-CERC-10-03, September 2010.

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