Michael Orshansky

Associate Professor
Electrical and Computer Engineering
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EDUCATION

University of California at Berkeley
Ph.D. Electrical Engineering, 2001
Dissertation: *Statistical Models, Methods, and Algorithms for Computer-Aided Design for Manufacturing*
Advisor: Prof. Chenming Hu

University of California at Berkeley
B.S. with Honors, Electrical Engineering and Computer Sciences, 1996

WORK EXPERIENCE

Department of Electrical and Computer Engineering, The University of Texas at Austin
Associate Professor, since August 2008

Department of Electrical and Computer Engineering, The University of Texas at Austin
Assistant Professor, 2003-2008

Gigascale Silicon Research Center, University of California at Berkeley
Research Scientist, November 2001-August 2003

Department of Electrical Engineering and Computer Sciences, UC Berkeley
Lecturer, Fall 2002

eSilicon Corporation, Santa Clara, CA
Member of Technical Staff, 2000-2001

HONORS AND AWARDS

- National Science Foundation CAREER Award, 2004
- ACM SIGDA Outstanding New Faculty Award, 2007
- Research Highlight in Communications of ACM, 2009
- IEEE/ACM William J. McCalla ICCAD Best Paper Award, 2006
- Best Paper Award, International Symposium on Quality Electronic Design, 2006
- Best Paper Award, Design Automation Conference, 2005
- Best Paper Award, IEEE Transactions on Semiconductor Manufacturing 2005

- ACM Recognition of Service Award, 2007
- Outstanding Service to IEEE Council on EDA Executive Committee, 2009
- University of Texas Faculty Research Award, 2004
- Best Paper in Session Award, Semiconductor Research Corporation Technical Conference, 2008
- Best Paper in Session Award, Semiconductor Research Corporation Technical Conference, 2007
- Best Paper in Session Award, Semiconductor Research Corporation Technical Conference, 2003
- Advanced Micro Devices Fellowship, 1998-2000
- Semiconductor Research Corporation Doctoral Fellowship, 1998-2000
- Listed in Marquis' "Who's Who in America," 2003-2007

RESEARCH CENTER PARTICIPATION:

- Gigascale Systems Research Center, a MARCO Focus Research Center on system design, 2004-2009
  - *Alternative Computational Models for Late and Post Silicon Technologies Theme*
  - *Resilient System Design Theme*

- Center for Circuits and Systems Solutions (C2S2), a MARCO Focus Research Center on circuit design, 2006-2009
  - *Silicon Infrastructure Theme*

PROGRAM COMMITTEE CHAIRMANSHIPS:

- Track Chair, Wild and Crazy Ideas
  - *Design Automation Conference*, 2011
- General Chair
  - *Austin Conference on Integrated Systems and Circuits* (ACISC), 2010
- General Chair
  - *ACM/IEEE International Workshop on Timing Issues in Digital Systems* (TAU), 2007
- Program Chair
  - *Austin Conference on Integrated Systems and Circuits* (ACISC), 2007
- Track Chair, Design for Manufacturability
  - *ACM/IEEE International Conference on Computer Aided Design* (ICCAD), 2007-2009
- Local Arrangements Chair
  - *IEEE Workshop on Silicon Errors in Logic - System Effects* (SELSE), 2008
- Track Chair, Logic and Circuit Design
  - *IEEE International Conference on Computer Design* (ICCD), 2005

MEMBERSHIP IN TECHNICAL PROGRAM COMMITTEES:

- *ACM/IEEE Design Automation Conference* (DAC), 2011
- *Workshop on Design for Manufacturability & Yield,* 2010
- *ACM/IEEE International Conference on Computer Aided Design* (ICCAD), 2009
- *Workshop on Design for Manufacturability & Yield,* 2009
- *IEEE/ACM Symposium on Nanoscale Architectures* (NANOARCH)*,* 2008
- *ACM/IEEE International Conference on Computer Aided Design* (ICCAD), 2008
- *Workshop on Design for Manufacturability & Yield,* 2008
- *IEEE/ACM Symposium on Nanoscale Architectures* (NANOARCH)*,* 2007
- *ACM/IEEE International Conference on Computer Aided Design* (ICCAD), 2007
- *Workshop on Design for Manufacturability & Yield,* 2007
- *ACM/IEEE Design Automation Conference* (DAC), 2006
- *ACM/IEEE International Conference on Computer Aided Design* (ICCAD), 2006
- *ACM/IEEE International Workshop on Timing Issues in Digital Systems* (TAU), 2006
- *IEEE International Conference on Computer Design*, 2006
- *Workshop on Design for Manufacturability & Yield,* 2006
- *IEEE Austin Conference on Systems and Circuits* (ACISC), 2006
- *ACM/IEEE Design Automation Conference* (DAC), 2005
- *IEEE International Conference on Computer Design*, 2005
- *ACM/IEEE Design Automation Conference* (DAC), 2004
- *IEEE International Conference on Computer Design*, 2004
- *ACM/IEEE International Workshop on Timing Issues in Digital Systems* (TAU), 2005

PROFESSIONAL ACTIVITIES AND SERVICE:

- Keynote Address at the *International On-Line Test Symposium*, Corfu Greece, 2010.
- National Science Foundation “Expeditions in Computing” Panel, March 2010.
- Keynote Address at the *2nd International Workshop on Design for Reliability and Variability (DRVW’09),* Austin, Texas, November 6, 2009.
- Panelist, Panel on “Design for Reliability: Too many ideas, too few tools,” *2nd International Workshop on Design for Reliability and Variability (DRVW’09),* Austin, Texas, November 6, 2009.
- Best Paper Award Committee Member, *IEEE/ACM Design Automation Conference (DAC)*, 2009
- Panelist, Managing Variation and Yield in Architectures and Applications, *Workshop on Design for Manufacturability & Yield,* 2009.
- Presenter at Workshop for Young Faculty in EDA, San Francisco, July 2009.
- National Science Foundation Design Automation Review Panel, March 2009.
- Best Paper Award Committee Member, *IEEE/ACM International Conference on Computer Aided Design* (ICCAD), 2008.
- Vice President, IEEE Council on Electronic Design Automation (CEDA), Technical Activities, 2008

- Chair of DFM Technical Committee of IEEE Special Interest Group on Design Automation (SIGDA), 2007
- Member of IEEE Council on Electronic Design Automation (CEDA) Technical Activities Committee, Organizer for Distinguished Speaker Series, 2007
- Associate Editor, *IEEE Transactions on Computer-Aided Design*, Modeling, Simulation and Validation
- Associate Editor, ACM Special Interest Group on Design Automation (SIGDA) E-Newsletter, 2006
- Reviewer for:
  - *IEEE Transactions on Computer-Aided Design*
  - *IEEE Transactions on VLSI Systems*
  - *IEEE Transactions on Circuits and Systems I*
  - *Journal of Solid-State Circuits*
  - *IEEE Transactions on Semiconductor Manufacturing*
  - *IEEE Transactions on Electron Devices*
  - *IEEE Electron Device Letters*
  - *IEEE Design and Test of Computers*
  - *ACM Transaction on Design Automation of Electronic Systems*
  - *Elsevier Integration*: *the VLSI Journal*
- Reviewer for *ACM Best Dissertation Award in EDA* in 2005
- Proposal reviewer for University of California MICRO program

UNIVERSITY COMMITTEE ASSIGNMENTS:

Member, EERC Building Committee	2010
TA Allocation/Planning Committee	since 2010
Co-Chair, Dept. of ECE, Undergraduate Curriculum Reform Committee	2008 – 2009
Member, Dept. of ECE, Faculty Incentives Program Committee	since 2009
Course Coordinator, Integrated Circuits and Systems Track	since 2007
Member, Dept. of ECE, EERC Planning Committee	2010
Member, Dept. of ECE, Student Appeals Committee	2003 - 2007
Member, Dept. of ECE, Circuit Design Track Faculty Search Committee	2004 - 2007
Member, Dept. of ECE, Graduate Studies Committee	2003 - 2007
Member, Dept. of ECE, Computer Engineering Graduate Admission committee	2003 - 2007

Member, Dept. of ECE, Committee on Graduate Student Financial Aid Reform	April - August 2007
Co-Chairman, VLSI Seminar Committee	2004 - 2007

COMMUNITY ACTIVITIES:

- HKN Fireside Chat, Spring 2008
- Student Technical Area Advising, HKN Technical Area Night, Spring 2006
- Prospective Graduate Student Visit Day organizer, Spring 2006
- Graduate Student Orientation Panelist, Fall 2006
- Co-Organizer, University of Texas VLSI Seminar series, 2003 – present

CONSULTING:

Patent Consulting, Moore Landrey, L.L.P.	2009-2010
Aprio Technologies	2006-2007
Blaze DFM	2007-present
Cambridge University Press	2004
eSilicon Corporation	2001-2003

PUBLICATIONS:

CITATION ANALYSIS:

The citation analysis is based on data from Google Scholar retrieved on 11/21/2010:

- Total citation count for 6 top cited papers: 1067
- Papers with more than 90 citations: 3 (highlighted below)
- Papers with more than 40 citations: 5

[436 citations] Y. Cao, T. Sato, M. Orshansky, D. Sylvester, and C. Hu, “New paradigm of predictive MOSFET and interconnect modeling for early circuit design,” *Proc. of IEEE Custom Integrated Circuits Conference (CICC)*, pp.201-4, Orlando, FL 2000.

[163 citations] M. Orshansky and K. Keutzer, “A General Probabilistic Framework for Worst Case Timing Analysis,” *Proc. of ACM/IEEE Design Automation Conference,* New Orleans, pp. 556-561, 2002.

[177 citations] M. Orshansky, L. Milor, P. Chen, K. Keutzer, and C. Hu, “Impact of Systematic Spatial Intra-Chip Gate Length Variability on Performance of High-Speed Digital Circuits,” *Proc. of IEEE/ACM International Conference on Computer Aided Design,* pp. 62-27, San Jose, CA, 2000.

BOOKS AND BOOK CHAPTERS:

[1] M. Orshansky, S. Nassif, D. Boning, *Design for Manufacturability and Statistical Design: A Constructive Approach*, Springer, January 2008.

[2] M. Mani and M. Orshansky, "Winning the power struggle in an uncertain era," *in* D. Chinnery and K. Keutzer, *Closing the Power Gap between ASIC and Custom*, Springer, 2007.

[3] M. Orshansky, “Increasing Circuit Performance through Statistical Design Techniques,” Chapter 14, of *Closing the Gap Between ASIC and Custom: Tools and Techniques for High-Performance ASIC Design*, D. Chinnery, K. Keutzer, Editors, Kluwer Academic Publishers, pp. 323-344, 2002.

[4] M. Orshansky, “Performance Penalty Imposed by the Tight Power Constraints of ASIC Designs,” in *Closing the Gap Between ASIC and Custom: Tools and Techniques for High-Performance ASIC Design*, D. Chinnery, K. Keutzer, Editors, Kluwer Academic Publishers, pp. 152-154, 2002.

JOURNAL ARTICLES:

[1] M. Orshansky and W. S. Wang, “Statistical Analysis of Circuit Timing Using Majorization,” *Communications of the ACM* (CACM), vol. 52, no. 8, August 2009.

[2] N. R. Shanbhag, S. Mitra, G. de Veciana, M. Orshansky, R. Marculescu, J. Roychowdhury, D. Jones and J. M. Rabaey, “*The Search for Alternative Computational Paradigms*,” *IEEE Design and Test*, vol. 25, no. 4, pp. 334-343, Jul. 2008.

[3] M. Mani, A. Devgan, M. Orshansky and Y. Zhan, "A Statistical Algorithm for Power- and Timing-Limited Parametric Yield Optimization of Large ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, vol. 26, no. 10, pp. 1790-1802, October 2007.

[4] W.S. Wang and M. Orshansky, "Estimation of Leakage Power Consumption and Parametric Yield Based on Realistic Probabilistic Descriptions of Parameters," *ASP Journal of Low Power Electronics*, vol. 3, no. 1, pp. 1-12, March 2007.

[5] K. Constantinides, S. Plaza, J. Blome, B. Zhang, V. Bertacco, S. Mahlke, T. Austin, M. Orshansky, “BulletProof: A Defect-Tolerant CMP Switch Architecture,” *ACM Transactions on Architecture and Code Optimization*, Vol. 4, No. 1, pp. 1-37, March 2007,

[6] W.-S Wang and M. Orshansky, "Path-based statistical timing analysis handling arbitrary delay correlations: theory and implementation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 12, pp. 2976-2988, December 2006.

[7] W. S. Wang, M. Liu, and M. Orshansky, “Analysis of Leakage Power Reduction in Dual-Vth Technologies in the Presence of Large Threshold Voltage Variation,” *ASP Journal of Low Power Electronics*, vol. 2, no. 1, pp. 1–7, March 2006.

[8] M. Orshansky, L. Milor, and C. Hu, “Characterization of spatial intra-field gate CD variability, its impact on circuit performance, and spatial mask-level correction,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 17, no. 1, pp. 2-11, February 2004*,* **Best Paper Award**.

[9] Y. Cao, M. Orshansky, D. Sylvester, T. Sato, and C. Hu, “SPICE up your MOSFET modeling: presenting a new paradigm of predictive MOSFET modeling for early circuit design innovation,” *IEEE Circuits and Devices Magazin*e, vol. 19, no. 4, pp. 17-23, July 2003.

[10] M. Orshansky, L. Milor, P. Chen, K. Keutzer, and C. Hu, “Impact of Systematic Spatial Intra-Chip Gate Length Variability on Performance of High-Speed Digital Circuits,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, vol. 21, no. 5, pp. 544-53, May 2002.

[11] M. Orshansky, J. An, C. Jiang, B. Liu, C. Riccobene, and C. Hu, “Efficient Generation of Pre-Silicon MOS Model Parameters for Early Circuit Design,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 1, pp.156-59, January 2001.

[12] M. Orshansky, J. C. Chen, and C. Hu, “Direct Sampling Methodology for Statistical Analysis of Scaled CMOS Technologies,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 12, no. 4, pp. 403-8, November 1999.

[13] D. Sinitsky, F. Assaderaghi, M. Orshansky, J. Bokor, and C. Hu, “Velocity Overshoot of Electrons and Holes in Si Inversion Layers,” *Journal of Solid-State Electronics,* vol. 41, no. 8, pp.1119-25, August 1997.

CONFERENCE ARTICLES:

[1] A. K. Singh, M. Lok, C. Caramanis and M. Orshansky, “An Algorithm for Exploiting Modeling Error Statistics to Enable Robust Analog Optimization”, *Proc. of International Conference on Computer-Aided Design*, 2010.

[2] M. Lok, K. He, M. Mani, C. Caramanis and M. Orshansky, “Design of Power-Optimal Buffers Tunable to Process Variability,” *IEEE Dallas Circuits and Systems Workshop,* 2010.

[3] S. Banerjee, K. Agarwal and M. Orshansky, “Ground Rule Slack Aware Tolerance-Driven Optical Proximity Correction for Local Metal Interconnects,” *Proc. of Custom Integrated Circuits Conference,* 2010.

[4] S. Banerjee, K. Agarwal and M. Orshansky, “Simultaneous Mask and Target Optimization for Improving Lithographic Process Window,” *Proc. of International Conference on Computer-Aided Design*, 2010.

[5] M. Basoglu, M. Erez, M. Orshansky, “NBTI-Aware DVFS: A New Approach to Saving Energy and Increasing Processor Lifetime,” *Proc. of IEEE International Symposium on Low-Power Design*, Austin, TT, August 2010.

[6] S. Banerjee, K. Agarwal and M. Orshansky, “Simultaneous Mask and Target Optimization for Improving Lithographic Process Window,” *Proc. of the 4th IEEE International Workshop on Design for Manufacturability and Yield*, Anaheim, CA, June 2010.

[7] S. Banerjee, K.B. Agarwal, C.-N. Sze, S. Nassif and M. Orshansky, *“*A Methodology for Propagating Design Tolerances to Shape Tolerances for Use in Manufacturing,” *Design Automation and Test in Europe*, pp. 1273-78, March 2010.

[8] A. K. Singh, K. He, C. Caramanis, and M. Orshansky, “Improved SRAM Design using Adaptive Architectures,” 4th Annual Austin Conference on Integrated Systems & Circuits, Oct 26-27, 2009.

[9] S. Banerjee, K. B. Agarwal, J. A. Culp, P. Elakkumanan, L. W. Liebmann, and M. Orshansky, “Leakage Minimization with Reduced Mask Cost using Electrically-Driven Optical Proximity Correction”, 4th Annual Austin Conference on Integrated Systems & Circuits, Oct 26-27, 2009.

[10] A. K. Singh, K. He, C. Caramanis, and M. Orshansky, “Mitigation of Intra-Array SRAM Variability using Adaptive Voltage Architecture,” *Proc. of IEEE/ACM International Conference on Computer Aided Design*, pp. 637-644, San Jose*,* 2009.

[11] S. Banerjee, K. B. Agarwal, J. A. Culp, P. Elakkumanan, L. W. Liebmann, and M. Orshansky, “Compensating non-optical effects using electrically driven optical proximity correction,” *Proc. of SPIE*, 7275, 2009.

[12] S. Banerjee, P. Elakkumanan, L. W. Liebmann and M. Orshansky, “Electrically Driven Optical Proximity Correction Based on Linear Programming”, *Proc. of IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, November, 2008.

[13] B. Zhang and M. Orshansky, "Modeling of NBTI-Induced PMOS Degradation under Arbitrary Dynamic Temperature Variation," *IEEE International Symposium on Quality Electronic Design* (ISQED), San Jose, CA, March 2008.

[14] S. Banerjee, P. Elakkumanan, D. Chidambarrao, J. Culp, S. Mukhopadhyay, and M. Orshansky, "A Systematic Variation Aware Circuit Simulation Engine," *SPIE Symposium on Advanced Lithography*, San Jose, CA, February 2008.

[15] A. K. Singh, H. Zeineddine, A. Aziz, S. Vishwanath, and M. Orshansky, "A Heterogeneous CMOS-CNT Architecture utilizing Novel Coding of Boolean Functions," *Proc. of IEEE/ACM Symposium on Nanoscale Architectures,* San Jose, CA, October 2007.

[16] A. Ramalingam, A. Singh, S. Nassif, M. Orshansky, D. Z. Pan, "Accurate Waveform Modeling using Singular Value Decomposition with Applications to Timing Analysis", *Proc. of ACM/IEEE Design Automation Conference*, pp. 148-153, San Diego, CA, June 2007.

[17] R. Tayade, S. Nassif, V. Kalyanam, M. Orshansky, and J. Abraham, "Estimating Path Delay Distribution Considering Coupling Noise," *Proc. of ACM Great Lake Symposium on VLSI*, pp. 61-66, Stresa-Lago Maggiore, Italy, April 2007.

[18] M. Mani, A. Singh, and M. Orshansky, "Joint Design-Time and Post-Silicon Minimization of Parametric Yield Loss using Adjustable Robust Optimization," *Proc. of IEEE/ACM International Conference on Computer Aided Design*, pp. 19-26, San Jose, CA, November 2006. **Best Paper Award.**

[19] B. Zhang, A. Arapostathis, S. Nassif, and M. Orshansky, "Analytical Modeling of SRAM Dynamic Stability," *Proc. of IEEE/ACM International Conference on Computer Aided Design*, pp. 315-322, San Jose, CA, November 2006.

[20] A. Ramalingam, A. K. Singh, S. Nassif, G.-J. Nam, D. Pan, and M. Orshansky, "An Accurate Sparse Matrix Based Framework for Statistical Static Timing Analysis," *Proc. of IEEE/ACM International Conference on Computer Aided Design*, pp. 231-236, San Jose, CA, November 2006.

[21] W.S. Wang and M. Orshansky, "Robust Estimation of Parametric Yield under Limited Variational Data," *Proc. of IEEE/ACM International Conference on Computer Aided Design*, pp. 884-890, San Jose, CA, November 2006.

[22] S. Banerjee, P. LoPresti, C. Wu, and M. Orshansky, "A Modeling Technique for Accurate Circuit Simulation of Non-Rectangular Gates," *Proc. of IEEE International Workshop on Design for Manufacturability and Yield*, San Jose, CA, October 2006.

[23] W. S. Wang, M. Orshansky, "Statistical Timing Based on Incomplete Probabilistic Descriptions of Parameter Uncertainty," *Proc. of ACM/IEEE Design Automation Conference*, pp. 161-166, San Francisco, CA, July 2006.

[24] A. Singh, M. Mani, R. Puri and M. Orshansky, "Gain-Based Technology Mapping for Minimum Runtime Leakage under Input Vector Uncertainty," *Proc. of ACM/IEEE Design Automation Conference*, pp. 522-527, San Francisco, CA, July 2006.

[25] M. Orshansky, “Statistical Minimization of Total Power under Timing Yield Constraints,” *in Proc. of IEEE International Conference on IC Design and Technology*, pp. 1-4, Padua, Italy, May 2006, **Invited.**

[26] M. Ceberio, M. Orshansky, G. Xiang, W. S. Wang, "Interval-Based Robust Statistical Techniques for Non-Negative Convex Functions, with Application to Timing Analysis of Computer Chips," *Proc. of ACM Symposium on Applied Computing*, pp. 1645-1649, Dijon, France, April 2006.

[27] J. Kim and M. Orshansky, "Towards Formal Probabilistic Power-Performance Design Space Exploration," *Proc. of ACM Great Lake Symposium on VLSI*, pp. 229-234, Philadelphia, PN, April 2006.

[28] M. Mani, M. Sharma, M. Orshansky, “Application of a Fast Statistical Sizing Algorithm based on Second Order Conic Programming in the Industrial Microprocessor Design Flow,” *Proc. of ACM Great Lake Symposium on VLSI*, pp. 372-375, Philadelphia, PN, April 2006.

[29] B. Zhang, W. Wang, and M. Orshansky, "FASER: Fast Analysis of Soft Error Susceptibility for Cell-Based Designs,” *Proc. of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 755-760, San Jose, CA, March 2006. **Best Paper Award**.

[30] K. Constantinides, S. Plaza, J. Blome, B. Zhang, V. Bertacco, S. Mahlke, T. Austin, M. Orshansky, “BulletProof: A Defect-Tolerant CMP Switch Architecture,” *Proc. of IEEE International Symposium on High Performance Computing and Applications*, pp. 3-14, Austin, Texas, February 2006.

[31] A. Singh, M. Mani, and M. Orshansky, “Statistical Technology Mapping for Parametric Yield,” *Proc. of IEEE/ACM International Conference on Computer-Aided Design*, pp. 511-518, San Jose, CA, November 2005.

[32] M. Mani, A. Devgan, and M. Orshansky, “An Efficient Algorithm for Statistical Minimization of Total Power under Timing Yield Constraints,” *Proc. of ACM/IEEE Design Automation Conference,* pp. 309-314, Anaheim, CA, June 2005. **Best Paper Award**.

[33] M. Mani and M. Orshansky, “A new statistical optimization algorithm for gate sizing,” *Proc. of IEEE International Conference on Computer Design*, pp. 272-277, San Jose, CA, October 2004.

[34] M. Liu, W.S. Wang, and M. Orshansky, “Leakage Power Reduction by Dual-Vth Designs under Probabilistic Analysis of Vth Variation,” *Proc. of IEEE International Symposium on Low-Power Design,* pp. 2-7, Monterey, CA, August 2004.

[35] M. Orshansky and A. Bandyopadhyay, “Fast Statistical Timing Analysis Handling Arbitrary Delay Correlations,” *Proc. of ACM/IEEE Design Automation Conference*, pp. 337-332, San Diego, CA, June 2004.

[36] M. Orshansky, “Fast computation of circuit delay probability distribution for timing graphs with arbitrary node correlation *Proc. of ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pp. 9-16, Austin, TX, February 2004.

[37] D. Nguyen, A. Davare, M. Orshansky, D. Chinnery, B. Thompson, and K. Keutzer, “Minimization of Dynamic and Static Power through Joint Assignment of Threshold Voltages and Sizing

Optimization," *Proc. of IEEE International Symposium on Low Power Design*, pp. 158-163, Seoul, Korea, August 2003.

[38] M. Orshansky and K. Keutzer, "A General Probabilistic Framework for Worst Case Timing Analysis," *Proc. of ACM/IEEE Design Automation Conference,* pp. 556-561, New Orleans, LN, June 2002.

[39] K. Keutzer and M. Orshansky, "From Blind Certainty to Informed Uncertainty," *Proc. of ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pp. 37-41, Monterey, CA, December 2002. **Invited.**

[40] M. Orshansky, L. Milor, P. Chen, K. Keutzer, and C. Hu, "Integration of Systematic Intra-Chip Gate Length Variability Into Timing Analysis," *Proc. of ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems,* pp. 39-44, Austin, TX, December 2000.

[41] M. Orshansky, L. Milor, P. Chen, K. Keutzer, and C. Hu, "Impact of Systematic Spatial Intra-Chip Gate Length Variability on Performance of High-Speed Digital Circuits," *Proc. of IEEE/ACM International Conference on Computer Aided Design,* pp. 62-27, San Jose, CA, November 2000.

[42] M. Orshansky, L. Milor, M. Brodsky, L. Nguyen, G. Hill, Y. Peng, and C. Hu, "Characterization of Spatial Intra-Field CD Variability," *Proc. of SPIE Conference on Optical Microlithography*, Vol. 4000, pp. 602-611, Santa Clara, CA, July 2000.

[43] Y. Cao, T. Sato, M. Orshansky, D. Sylvester, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," *Proc. of IEEE Custom Integrated Circuits Conference (CICC)*, pp. 201-4, Orlando, FL, May 2000.

[44] M. Orshansky, L. Milor, L. Nguyen, G. Hill, Y. Peng, and C. Hu, "Intra-Field Gate CD Variability and Its Impact On Circuit Performance," *Proc. of IEEE International Electron Devices Meeting*, pp. 479-82, Washington D.C., December 1999.

[45] M. Orshansky, C. Spanos, and C. Hu, "Circuit Performance Variability Decomposition," *Proc. of IEEE International Workshop on Statistical Metrology for VLSI Design and Fabrication*, pp. 10-13, Kyoto, Japan, June 1999.

[46] M. Orshansky, J. Chen, C. Hu, C-P. Wan, P. Bendix, "Approaches to Statistical Circuit Analysis for Deep Sub-Micron Technologies," *Proc. of IEEE International Workshop on Statistical Metrology for VLSI Design and Fabrication*, pp. 6-9, Honolulu, Hawaii, June 1998.

[47] M. Orshansky, J. Chen, and C. Hu, "A Statistical Performance Simulation Methodology for VLSI Circuits," *Proc. of ACM/IEEE Design Automation Conference*, pp. 402-7, San Francisco, CA, June 1998.

[48] M. Orshansky, D. Sinitsky, P. Scrobohaci, J. Bokor, and C. Hu, "Impact of Velocity Overshoot, Polysilicon Depletion, and Inversion Layer Quantization on NMOSFET Scaling," *Proc. of IEEE Device Research Conference*, pp. 18-19, Charlottesville, VI, June 1998.

[49] J. Chen, M. Orshansky, C. Hu, C-P. Wan, P. Bendix, "Statistical Circuit Characterization for Deep-Submicron CMOS Designs," *Proc. of IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 90-91, San Francisco, CA, February 1998.

[50] W. Liu, M. Orshansky, X. Jin, K. Chen, and C. Hu, "MOSFET Intrinsic-Capacitance Related Inaccuracy in CMOS Circuit Speed Simulation," *Proc. of IEEE International Semiconductor Device Research Symposium*, pp. 337-340, Charlottesville, VI, December 1997.

[51] D. Sinitsky, F. Assaderaghi, M. Orshansky, J. Bokor, C. Hu, "An Extension of BSIM3 Model Incorporating Velocity Overshoot," *Proc. of IEEE International Symposium on VLSI Technology, Systems, and Applications*, pp. 307-310, Taipei, Taiwan, June 1997.

OTHER PUBLICATIONS (UNPUBLISHED REFEREED WORKSHOP NOTES):

[1] A. K. Singh, M. Orshansky, “Logic Synthesis for Reducing Leakage Power Consumption under Workload Uncertainty,” 12 WSEAS Conference on Circuits, July 2008.

[2] S. Banerjee, P. Elakkumanan, L. W. Liebmann and M. Orshansky, “Electrically Driven Optical Proximity Correction Based on Linear Programming”, *Proc. of SRC Technical Conference*, Sept. 2008, **Best Paper in Session Award**.

[3] M. Mani, A. K. Singh, and M. Orshansky, "Parametric Yield Loss Reduction Using Adjustable Robust Optimization," *Proc. of SRC Technical Conference*, Sept. 2007, **Best Paper in Session Award**.

[4] A. Ramalingam, A. Singh, S. Nassif, M. Orshansky and D. Pan, "Accurate Waveform Modeling using Singular Value Decomposition with Applications to Timing Analysis," *Proc. of Timing Analysis Workshop*, February 2007.

[5] W. S. Wang, M. Orshansky, "Robust Timing Analysis under Uncertainty for Timing Sign-Off," *Proc. of Timing Analysis Workshop*, San Francisco, CA, February 2006.

[6] M. Orshansky and W.S. Wang, G. Xiang and V. Kreinovich, “Interval-Based Robust Statistical Techniques for Non-Negative Convex Functions, with Application to Timing Analysis of Computer Chips,” *Second workshop on Reliable Engineering Computing Georgia Institute of Technology*, February 22-24, Savanna, GA, 2006.

[7] K. Constantinides, S. Plaza, J. Blome, B. Zhang, V. Bertacco, S. Mahlke, T. Austin, M. Orshansky, “Assessing SEU Vulnerability via Circuit Level Timing Analysis,” *Workshop on Architectural Reliability (WAR-1)*, Barcelona, Spain, November 2005.

[8] B. Zhang and M. Orshansky, “SER Prediction by Symbolic Simulation of the Propagation and Filtering of Transient Faulty Pulses,” *Workshop on System Effects of Logic Soft Errors*, Urbana-Champaign, IL, March 2005.

[9] D. G. Chinnery, B. Thompson, M. Orshansky, K. Keutzer, “Power Minimization with Multiple Supply Voltages and Multiple Threshold Voltages,” *Proc. of SRC Technical Conference*, Dallas, 2003. **Best Paper in Session Award.**

TECHNICAL REPORTS:

[1] A. Singh, A. Aziz, M. Orshansky, S. Vishwanath, "Generation of Efficient Codes for Realizing Boolean Functions in Nanotechnologies," *Technical Report*, WNCG-TR-2007-02-01, 2007.

[2] M. Mani, C. Caramanis, and M. Orshansky, "Power Efficient Memory Design under Variability using Finite Adaptable Optimization," *Technical Report*, WNCG-TR-2007-07-09, 2007.

ORAL PRESENTATIONS:

[1] Institute for Pure and Applied Mathematics Robust Optimization Workshop, *Invited,* “Applications of Robust Optimization in Integrated Circuit Design”, UCLA, November 2010.

[2] AMD, “Adaptivity for Low Power Design,” Austin, Texas, July 30, 2010.

[3] Keynote Address, “Statistical Design of Digital Circuits: the First Ten Years,” *16th IEEE International On-Line Testing Symposium*, Corfu Island, Greece, July 5-7, 2010

[4] Intel Circuit Research Labs, “Using Adaptivity to Enable Robust Low-Power Design,” Hillsborough, Oregon, April 2010.

[5] Keynote Address, “Statistical Design on the Verge of Maturity: Revisiting the Foundation,” *2nd International Workshop on Design for Reliability and Variability (DRVW'09),* Austin, Texas, November 6, 2009.

[6] Asia-South Pacific Design Automation Conference, “Statistical Design on the Verge of Maturity: Revisiting the Foundation,” Half-Day Tutorial Presenter, January 2009.

[7] M. Orshansky, “Design of Power-Optimal Buffers Tunable to Process Variability,” IBM Austin Research Lab, 10/7/2008.

[8] M. Orshansky, "Optimization Strategies for Joint Design-Time and Post-Silicon Tuning for Yield," Advanced Micro Devices, May 29, 2008.

[9] M. Orshansky, "Design Optimization for Robustness," EECS Seminar, University of California, Berkeley, February 26, 2008.

[10] M. Orshansky, "Statistical Design Methods for Power Reduction and Yield Improvement," UT ECE Research Review for Industry, August 28, 2007, Austin.

[11] International Conference on Computer Aided Design (ICCAD), Half-day tutorial co-presenter, "Post-Silicon Adaptivity for Yield Improvement," November 5, 2007, *invited.*

[12] M. Orshansky, "Improvement of Power-Limited Parametric Yield using Adjustable Robust Optimization", Synopsys Engineering Seminar Series (SESS), Mountain View, CA, July 2007.

[13] Sun Microsystems, "Low Power Optimization under Variability," Austin, TX, November 1, 2007, *invited.*

[14] University of Minnesota, Minneapolis, "Use of Coding for Low-Level Defect Tolerance," October 18, 2007, *invited.*

[15] Design Automation Summer School, "Statistical Design and Optimization," San Diego, CA, June 3, 2007*, invited*.

[16] University of California, Los Angeles, "Statistical Design Techniques for Digital ICs," June 1, 2007*, invited*.

[17] Distinguished Seminar Series, IEEE Council on Electronic Design Automation, "Joint Design-Time and Post-Silicon Minimization of Parametric Yield Loss using Adjustable Robust Optimization," Berkeley, CA, January 2, 2007*, invited*.

[18] External Long-Range Research Symposium, Intel Corporation, "Self-Healing and Resilient Systems," San Jose, August 28, 2006*, invited*.

[19] Freescale, "Power-Limited Parametric Yield Optimization and Timing Analysis under Incomplete Description of Uncertainty," Austin, Texas, August 23, 2006*, invited*.

[20] Synopsys, "Timing Analysis under Incomplete Description of Uncertainty," Hillsboro, Oregon, August 16, 2006*, invited*.

[21] Intel Corporation, Strategic CAD Labs, "Optimization Techniques for Power-Limited Parametric Yield Improvement and Timing Analysis under Incomplete Description of Uncertainty," Hillsboro, Oregon, August 16, 2006*, invited*.

[22] International Symposium on Quality of Electronic Design (ISQED 2006), Full-day tutorial co-presenter, "Variability and Its Impact on Design," San Jose, CA, March 2006*, invited*.

[23] Design Automation and Test in Europe Conference (DATE), Full-day tutorial co-presenter, "Statistical Design Optimization Techniques," Munich, Germany, March 2006*, invited*.

[24] Asia and South Pacific Design Automation Conference (ASP-DAC) 2006, Full-day tutorial co-presenter, "DFM Tools and Methodologies for 65nm and below," Yokohama, Japan, January 2006*, invited*.

[25] National Taiwan University, "Statistical Performance Analysis and Optimization," Taipei, Taiwan, December 2005*, invited*.

[26] Panelist, Manufacturing for Design meets Design for Manufacturing Forum, Semiconductor Research Corporation, Santa Clara, CA, October 2005*, invited*.

[27] International Conference on Integrated Circuits, Devices, and Technology (ICICDT), "Statistical Minimization of Total Power under Timing Yield Constraints," Padua, Italy, May 2006*, invited*.

[28] National Tsing Hua University, "Statistical Performance Analysis and Optimization," Hsinchu, Taiwan, December 2005*, invited*.

[29] Design Automation Conference, Full-day tutorial co-presenter, "Statistical Performance Analysis and Optimization of Digital Circuits," Anaheim, CA, June 2005*, invited*.

[30] Silicon Integration Initiative (SI2), Austin, TX, June 2006*, invited*.

[31] Silicon Design Systems, "Opportunities in DFM," Austin, TX, December 2005*, invited*.

[32] Stratospheric Solutions, "Statistical Circuit Analysis and Design," Austin, TX, May 2005*, invited*.

[33] Advanced Micro Devices, “Towards a Low Power Design Methodology under Variability: Statistical Modeling, Analysis, and Optimization,” Austin, TX, June 2005*, invited*.

[34] IBM T.J. Watson Research Center, Design Automation Professional Interest Community Seminar, “Towards a Low Power Design Methodology under Variability: Statistical Modeling, Analysis, and Optimization,” May 2005*, invited*.

[35] Intel Corporation, Strategic CAD Labs, “Towards Developing a Statistical Design Methodology: Statistical Circuit Modeling, Timing Analysis and Gate Sizing,” Hillsboro, Oregon, September 2004*, invited*.

[36] ANOVA Solutions, “Towards a Low Power Design Methodology under Variability: Statistical Modeling, Analysis, and Optimization,” Santa Clara, CA, June 2005*, invited*.

[37] Synopsis Strategic Technical Offsite, “Statistical Design in Nanometer CMOS: CAD perspective,” Monterey, CA, March 2005*, invited*.

[38] University of Michigan, Micron Technology VLSI Seminar Series, “Towards Developing a Statistical Design Methodology: Statistical Circuit Modeling, Timing Analysis and Gate Sizing,” Ann Arbor, MI, December 2004*, invited*.

[39] IBM Austin Research Laboratory, "Robust Circuit Design and Statistical STA,” Austin, TX, October 2003*, invited*.

[40] Motorola, Computer-Aided Design Group, "Statistical Timing Analysis Methods," April 2004, Austin, TX*, invited*.

[41] Gigascale Silicon Research Center, "Techniques for Probabilistic Design and Probabilistic Design Space Exploration," San Diego, CA, June 2004*, invited*.

[42] Berkeley Wireless Research Center, "Design for Manufacturability and Resolution Enhancement Techniques for Reliable IC Design," Berkeley, CA, July 2002*, invited*.

[43] Illinois Center for Integrated Microsystems, "Statistical Modeling for Computer-Aided Design for Manufacturing," Dept. of ECE, Urbana-Champaign, IL, September 2001*, invited*.

[44] Princeton University, "Statistical Methods and Models for Design for Manufacturing," Dept. of Electrical Engineering, Princeton, NJ, April 2001*, invited*.

[45] Semiconductor Research Corporation Technical Conference, "Intra-Field Gate CD Variability and Its Impact on Circuit Performance," Austin, TX, September 1999*, invited*.

PATENTS:

Patents Issued:

1. Klaus ten Hagen and Michael Orshansky, "An Adaptive Real-Time Work-in-Progress Tracking, Prediction, and Optimization System for a Semiconductor Supply Chain," U.S. Patent 6,748,287, Granted 6/8/2004.

2. M. Orshansky and M. Mani, "Method for performing post-synthesis circuit optimization, U.S. Patent 7,665,047, Granted 2/16/2010.

GRANTS AND CONTRACTS:

Co-Investigators	Title	Agency	Grant Total (My Share)	Grant Period
Gerstlauer Orshansky	Formal Synthesis of Low-Energy Signal Processing Systems Relying on Controlled Timing-Error Acceptance	National Science Foundation	$450,000 ($225,000)	9/1/10-8/31/13
Orshansky (PI)	CAREER: Tools for Design for Manufacturability in Nanometer CMOS	National Science Foundation	$400,000	8/1/04-7/31/09
Orshansky (PI) Sylvester (U.Michigan)	Formal Design Techniques for Adaptive Circuit Fabrics	National Science Foundation	$464,000 ($280,000)	8/1/06-8/1/09

Orshansky (PI)	Construction of Noise-Resilient Circuits from Unreliable Gates and Monitoring and Diagnosis Framework for On-Line System Reliability Tuning	Gigascale Systems Research Center (GSRC), MARCO Focus Research Center	$300,000	9/1/06-8/31/09
Pan (PI) Orshansky	Unified Treatment of Systematic and Random Variations for Analysis/Optimization with Variational Litho-Modeling	Semiconductor Research Corporation	$390,000 ($195,000)	7/1/06-6/31/09
Orshansky (PI)	Circuit Synthesis under Uncertainty using Design-Time Optimization and Post-Fabrication Adaptivity	Center for Circuits, Systems, and Software (C2S2), MARCO Focus Research Center	$164,000	9/1/06-8/31/09
Orshansky (PI)	System-Level Living Roadmap	Gigascale Systems Research Center (GSRC), MARCO Focus Research Center	$230,000	9/01/04-8/31/06
Orshansky (PI) Jacome	A Formal Methodology for Probabilistic Design of Robust Nanometer Scale Digital Circuits	Semiconductor Research Corporation	$225,000 ($175,000)	10/1/04-9/31/07
Orshansky (PI)	Robust Circuit Design and Design Automation	Intel Corporation	$35,000	2005
Orshansky (PI)	Research equipment grant to support research on variability	Sun Microsystems	$35,000	2004
TOTAL			$2.24M ($1.81M)	

PH.D. SUPERVISIONS COMPLETED:

Wei-Shen Wang	Algorithms for Statistical Timing and Power Analysis of Digital Integrated Circuits	May 2007	ECE	Univ. of Texas at Austin
Ashish Singh	Robust Circuit Synthesis	September 2007	ECE	Univ. of Texas at Austin
Bin Zhang	IC Design for Reliability	December 2008	ECE	Univ. of Texas at Austin

Murari Mani	Robust Algorithms for Area and Power Optimization of Digital Integrated Circuits under Variability	December 2008	ECE	Univ. of Texas at Austin
Shayak Banerjee	Enhancing the Design - Manufacturing Interface in Nanoscale Technologies	May 2010	ECE	Univ. of Texas at Austin

M.S. SUPERVISIONS COMPLETED:

Shayak Banerjee	Electrical Modeling of Non-Rectangular Gates	May 2007	Electrical and Computer Engineering	Univ. of Texas at Austin
Murari Mani	Statistical Gate Sizing	December 2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Aniket Saha	Advanced Nanometer Circuit Design Techniques	December 2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Joonsoo Kim	Hierarchical Formal Probabilistic Power-Performance Design Space Exploration	December 2005	Electrical and Computer Engineering	Univ. of Texas at Austin
Hady Zeineddine	Coding for Circuit Fabrics with High Defect Densities	May 2009	Electrical and Computer Engineering	Univ. of Texas at Austin
Mario Lok	Process Variation Aware Low Power Buffer Design	May 2010	Electrical and Computer Engineering	Univ. of Texas at Austin

PH.D. DISSERTATION COMMITTEES:

1. Ajay Manohar Joshi, "Evaluating and Improving Workload Synthesis for Microprocessor Performance Evaluation"
2. Stephen Bijansky, "Asynchronous design for dealing with variability"
3. Baker Mohammad, "Cache Design for Low Power and Yield Enhancement"
4. Bassam Mohd, "Energy-Efficient Switch-Based Radix-2 Fast Fourier Transform Processor"
5. Rajeshwary Tayade, " Incorporating the Effect of Delay Variability in Path Based Delay Testing"
6. Anand Rajaram, "Design and Optimization of Variation Tolerant Clock Networks"
7. Tao Lou, "Nanometer VLSI Placement and Optimization for Multi-Objective Design Closure"
8. Anand Ramalingam, "Techniques for Path-Based Statistical Timing Analysis"

9. Murari Mani, "Robust Techniques for Area and Power Optimization of Digital Integrated Circuits under Variability"
10. Sundareswaran Savithri, "Improving Accuracy of Statistical Timing Analysis”
11. Ashish Singh, "Technology Mapping for Parametric Yield"
12. Wei-Shen Wang, "Models and Algorithms for Statistical Timing and Power Analysis of Digital Integrated Circuits"
13. Hani Saleh, “Fused Floating-Point Arithmetic for Digital Signal Processing”
14. Xiao Pu, “Bandwidth-enhanced Fractional-N PLL”
15. Sean Shi, “Modeling and Optimization to Connect Nanoscale Layout with Silicon”
16. Andrey Zykov, “Exploring Scaling Limits and Computational Paradigms for Next Generation Embedded Systems”
17. Kun Yuan, “Physical Design Automation for Double Patterning Lithography”
18. Tung-Yeh Wu, “Strategies against Power Supply Noise – from Estimation, Reduction, to Detection”
19. Jaeyong Chung, “Graph decomposition methods in SSTA”
20. Sungmin Ock, “Highly linear transmitter”
21. Diptendu Ghosh, “Low Power Design Techniques for Radio Receiver Applications”
22. Jae-Seok Yang, “Nanometer VLSI Design-Manufacturing Interface for Large Scale Integration”
23. James (Yong Chan) Ban, “Modeling and Characterization of Contact-Edge Roughness”
24. Sriram Sambamurthy, “Power estimation of microprocessors”
25. Akram Waqas, “Design of High-Speed Arithmetic Blocks”
26. Jason Shih-Hsin Hu, “Reliable and Energy-Efficient Digital System Design”