Curriculum Vitae

Leonard Franklin Register II

TITLE: Full Professor
DEPARTMENT: Electrical and Computer Engineering (and Microelectronics Research Center)
UNIVERSITY: The University of Texas at Austin

EDUCATION:

North Carolina State University	Electrical Engineering	B.S. (summa cum Laude)	Spring 1983
North Carolina State University	Physics	B.S. (summa cum Laude)	Spring 1983
North Carolina State University	Elec. & Comp. Eng.	Ph.D.[1]	Spring 1990[2]

ACADEMIC POSITIONS:

The University of Texas at Austin	Full Professor (elect)	Fall 2011-present
The University of Texas at Austin	Temple Foundation Faculty Fellow, #4	Fall 2006-present
The University of Texas at Austin	Associate Professor	Fall 2005-Summer 2011
The University of Texas at Austin	Assistant Professor	Spring 2000-Summer 2005
University of Illinois at U-C	Research Scientist	Spring 1993-Fall 1999
University of Illinois at U-C	Visiting Research Assistant Prof.	Spring 1990-Fall 1992

VITA

Leonard Franklin Register is an Associate Professor of Electrical and Computer Engineering at the University of Texas at Austin, a member of the Microelectronics Research Center, and recipient of the Temple Foundation Endowed Faculty Fellowship #4. He has B. S. degrees both in Electrical Engineering and in Physics, and a Ph. D. in Electrical and Computer Engineering, each from North Carolina State University. He was a research scientist in the Computational Electronics group within the Beckman Institute at the University of Illinois at Urbana-Champaign before joining the faculty of The University of Texas at Austin in 2000. Prof. Register is a device theorist whose research is focused on understanding and modeling the essential physics underlying the operation of nanoelectronic and optoelectronic devices. His current research interests included alternative materials and device geometries for CMOS (non-classical CMOS), alternative switching methods and/or state variables (beyond CMOS), quantum-corrected semiclassical transport, and quantum transport with scattering. He is also published in areas including CMOS reliability, compact modeling, lasers, scattering theory and single electron devices.

[1] Michael A. Littlejohn, Advisor. Major area of study: Solid State Electronics; Minor areas of study: Electromagnetics, Communications and Physics; Research plus 54 hours of formal course work required
[2] Defended, January 1990.

HONORS AND AWARDS:

Temple Foundation Faculty Fellowship #4, The University of Texas at Austin, Fall 2006-present
Semiconductor Research Corporation (full) Fellowship, North Carolina State University, 1986-1990.
Microelectronics Center of NC (1 year full) Fellowship, North Carolina State University, 1983-1984.

POST-DOCTORAL SUPERVISIONS

Wanqiang Chen	1/2005-9/2006
Matthew Gilbert (W/Banerjee)	7/2005-5/2008

Ph.D. SUPERVISIONS (all in Electrical and Computer Engineering at UT-Austin)

COMPLETED

Yang-Yu Fan (w/ Banerjee)	2002
Wanqiang Chen	Fall 2004
Tongsheng Xia (w/ Banerjee)	Spring 2005
Fei Li (with Banerjee)	Spring 2006
Xiao-Feng Fan (w/ Banerjee)	Fall 2006
Bahniman Ghosh (w Banerjee)	Spring 2007
Xin Zheng Ph.D.	Fall 2007
Ken-Ming Liu	Summer 2008
Dipanjan Basu (w/ Banerjee)	Fall 2010

IN PROGRESS

Mohammad Mehedi Hasan	in candidacy
Ning-Yu Shi	in candidacy
Hui Chen	in candidacy
John David (w/ Banerjee)	in candidacy
Dharmendar Reddy	
Xuehao Mou	
Amithraj Valsaraj	
Jiwon Chang (w/ Banerjee)	
Priyamvada Jadaun, ECE (w/ Banerjee)	
Dax Crum, ECE (w/ Banerjee)	

M.S. SUPERVISIONS (all in Electrical and Computer Engineering at UT-Austin)

James Michael Flaherty	2003
Xin Zheng: M.S.	2003
Mohammad Mehedi: M.S.	2007
Ningyu Shi: M.S.	2007

OTHER ADVISING

SSE Area Advisor for graduate students, Fall 2001-Summer2011
SSE Area Coordinator for graduate students, Fall 2001-Summer2011
Departmental Graduate Advisor, Fall 2011-present

TEACHING (formal courses)

EE 339[3]	Introduction to Semiconductor Devices	undergraduate
EE325[4]	Electromagnetic Engineering	undergraduate
EE396K, Topic 2[5]	Semiconductor Physics	graduate
EE396V/Phy392T/CHE383[6]	Inorganic Nanostructures for Device applications	graduate (team)

UNIVERSITY COMMITTEES

University	Calendar Committee	Chair	2004-2005
	Calendar Committee	Member	2003-2004
	Faculty Review Committtee[7]	Member	2 times
Department	SSE track Graduate Admission Committee	Chair	2001-present
	Student Appeals Committee (undergraduate)	Member	2003-2006

EXTERNAL COMMITTEES AND OTHER SERVICE

INTERNATIONAL SOCIETIES

Technical Committee on Simulation and Modeling (TC-10) of the IEEE Nanotechnology Council, Fall 2006-present

INTERNATIONAL CONFERENCE COMMITTEES, SESSION ORGANIZER

Symposium Co-Chair for Nanoelectronic Devices, *Nanotech 2010* (Boston, MA, June 13-16, 2011.)
Program Committee, International Workshop on Computational Electronics (Pisa, Italy, October 27-29, 2010)
Symposium Co-Chair for Nanoelectronic Devices, *Nanotech 2010* (Anaheim, Ca, June 21-25, 2010)
Symposium Co-Chair for Nanoelectronic Devices, *Nanotech 2009* (Houston, Texas, May 3-7, 2009)
Program Committee for *IEEE-NANO* 2009, Genoa, Italy, July 26-30, 2009. (as part of IEEE Nanotechnology Council, TC 10 duties)
Program Committee for *IEEE-NANO* 2007, Hong Kong (as part of IEEE Nanotechnology Council, TC 10 duties)
Program Committee and session organizer for *International Electron Devices Meeting (IEDM),* 2003 and 2004
Program Committee and session organizer for the *Device Research Conference (DRC)* 2001, 2002 and 2003
Program committee and session organizer for the *University, Government, Industry MEETING (UGIM), 2003*
Program committee for the *International Workshop on Computational Electronics (IWCE),* 2001

INTERNATIONAL CONFERENCE SESSION CHAIR

[3] Fall 2000, Fall 2001, Fall 2002, Fall 2003, Spring 2004, Fall 2004, Fall 2005 (2 sections), Fall 2006 (2 sections), Fall 2007 (2 sections), Fall 2008 (2 sections), Fall 2009, Fall 2010, Fall 2011
[4] Spring 2010.
[5] Spring 2001, Spring 2002, Spring 2003, Spring 2004, Spring 2005, Spring 2006, Spring 2007, Spring 2008, Spring 2009, Spring 2010, (Spring 2011 scheduled)
[6] Spring 2008, Spring 2009, Spring 2010 (Spring 2011 scheduled)
[7] Committee charged with reviewing performance of all faculty within department and reporting back to the Chair of ECE.

Session-Chair for Nanoelectronic Devices, *Nanotech 2010* (Boston, MA, June 13-16, 2011.)
Multi-session chair for *Nanotech 2010* (Anaheim, Ca, June 21-25, 2010)
Session-Chair for the *Electrochemical Society Meeting,* Vancouver, Canada, April 26-30th, 2010
Multi-session chair for *Nanotech 2009* (Houston, Texas, May 3-7, 2009)
Session chair for the *International Electron Devices Meeting (IEDM),* 2003, 2004
Session chair for the *University, Government, Industry MEETING (UGIM),* 2003
Session chair for *IEEE Conference on Nanotechnology (IEEE-Nano),* 2002
Session chair for the *International Workshop on Computational Electronics (IWCE),* 2001

REFEREEING FOR INTERNATIONAL JOURNALS (Partial list)

IEEE Electron Device Letters (Golden List of Reviewers)
IEEE Transactions on Electron Devices (Golden List of Reviewers)
IEEE Nanotechnology Letters
IEEE Transactions on Nanotechnology
Applied Physics Letters
Journal of Applied Physics
Physical Review Letters
Physical Review B
Journal of Computational Electronics

SPONSORED RESEARCH

Approximately $16,0360,00 worth of total awards with $3,754,000 for share spread over 24 individual or joint research contracts.

DISCLOSURES AND PATENTS

1. L. F. Register and S. K. Banerjee, **"**Hetero-barrier Tunnel Field-Effect Transistor (HetTFET) for low voltage logic," Disclosure, May 2008.
2. L. F. Register and S. K Banerjee, "Resonant Injection Enhanced Field-Effect Transistor (RIEFET)," Disclosure, May 2008. Patent 12/370,844, filed 2/13/09. Pending.
3. S. K Banerjee, Leonard F. Register, Emanuel Tutuc, Allan McDonald, and Dharmendar Reddy, "Bilayer Pseudo-Spin Field Effect Transistor (BiSFET)," Disclosure, August 2008. Provisional patent 61/118,251, filed 11/26/08. Non provisional patent 12/624,481 filed 11/24/2009. Pending.
4. Disclosure: Sanjay K Banerjee, Allan MacDonald, Leonard Franklin Register and Bhagawan R. Sahu, "BiSFETs and Novel Transistors based on Topological Insulators," Disclosure, 1/2011.

PUBLICATIONS

BOOK CHAPTERS

1. L. F. Register and S. K. Banerjee,."Bilayer pseudoSpin Field Effect Transistor (BiSFET)" in "Beyond CMOS Logic Switches," Ed. Kelin Khun and Tsu-Jae King Liu. In preparation.
2. Y.-Y. Fan, S. Mudanai, W. Chen, L. F. Register. S. K. Banerjee, "High-K Gate Dielectric Materials and Alternate Gate Electrode Integrated Circuit Design Issues" in High-K Gate Dielectric Materials for VLSI MOSFET Applications, Editors: Howard R. Huff and David C. Gilmer, (Springer-Verlag, 2003).
3. Y.-Y. Fan, S. Mudanai, W. Chen, L. F. Register. S. K. Banerjee, "High-K Gate Dielectric Materials and Alternate Gate Electrode Integrated Circuit Design Issues" in *High-K Gate Dielectric*

Materials for VLSI MOSFET Applications, Editors: Howard R. Huff and David C. Gilmer, (Springer-Verlag, 2003).

4. L. F. Register, W. Chen, X. Zeng and M. Stroscio, "Carrier Capture and Transport within Tunneling Injection Lasers: a Quantum Transport analysis" in *Selected topics in Electronics and Systems, vol. 28: Advanced Semiconductor Heterostructures* ," (World Scientific, 2003) pp. 197-207; the International Journal of High-Speed Electronics and Systems, 12, 1135-1145 (2002).
5. Leonard F. Register and Björn Fischer, "Collision Broadening Through Sequences of Scattering Events: Theory, Consequences and Modeling Within Semiclassical Monte Carlo" in *Selected Topics in Electronics and Systems; Topics in High Field Transport in Semiconductors*, " ed. K. F. Brennan, P Paul Ruden (World Scientific, 2001) pp 455-477.
6. Leonard F. Register, "Carrier Capture in Semiconductor Quantum Wells: A Quantum Transport Analysis" in Selected Topics in Electronics and Systems, Vol. 16: Advances in Semiconductor Lasers and Applications to Optoelectronics (2000, World Scientific, Singapore), pp 365–388.
7. K. Hess, L. F. Register, B. Tuttle, J. Lyding, and I. C. Kizilyalli, "Hot Carrier Degradation Issues in Submicron MOSFETs," *Future Trends in Microelectronics,* edited by S. Luryi, J. Xu and A. Zaslavsky, (1999, John Wiley & Sons, Inc.).
8. L. F. Register, "Schrodinger Equation Monte Carlo: bridging the Gap from Quantum to Classical Transport," in *Quantum-Based Electronic Devices and Systems*, vol. 14, *Selected Topic in Electronics and Systems*, M. Dutta and M. A. Stroscio, Eds.: World Scientific, Singapore, 1998, pp. 251-279.

REFEREED ARCHIVAL JOURNAL

9. (Jiwon Chang, Priyamvada Jadaun, Leonard F. Register, Sanjay K. Banerjee, and Bhagawan Sahu, "Dielectric capping effects on the topological insulator Bi2Se3 surface states", Phys. Rev. B, in review.)
10. (Priyamvada Jadaun, Sanjay K. Banerjee, Leonard F. Register, Bhagawan Sahu, "Density functional theory based study of graphene and dielectric oxide interfaces," Journal of Physics: Condensed Matter, in review.)
11. (John K. David, Leonard F. Register and Sanjay K. Banerjee, A Semi-Classical Monte Carlo Analysis of Graphene Field Effect Transistors, Transactions on Electron Devices, in review at time of writing.)
12. (Ningyu Shi, Leonard F. Register, and Sanjay K. Banerjee, "Strain, Surface Roughness and Valley-Dependent Quantum Confinement in Short-Channel n MOSFETs: a semiclassical Monte Carlo Study," IEEE Transactions on Electron Devices, *in revision at time of writing*.)
13. (Hui, Chen, Leonard F. Register, and Sanjay K. Banerjee, "Resonant Injection Enhanced Field Effect Transistor for Low-Voltage Switching: Concept and Simulation," Journal of Computational Electronics, *in revision at time of writing*)
14. John K. David, Leonard F. Register and Sanjay K. Banerjee, A Path Sum Monte Carlo Approach for Many-Electron Systems within a Tight-Binding Basis, Journal of Computational Electronics, *accepted for publication at time of writing*.
15. Leonard F. Register and Ningyu Shi, "Schrödinger-Equation-Based Quantum Corrections Addressing Degeneracy-Breaking and Confinement-Enhanced Scattering," Special Issue of the Journal of Computational Electronics on "From Compact to Atomistic Scale Modeling," *accepted for publication at time of writing* (**Invited** journal paper).
16. Leonard F. Register, Dipanjan Basu and Dharmendar Reddy, "From Coherent States in Adjacent Graphene Layers toward Low-Power Logic Circuits," special issue in Advances in Condensed Matter Physics on "Coherent States in Double Quantum Well Systems," *accepted for publication at time of writing.* (**Invited** journal paper).
17. Dipanjan Dipanjan. Basu, Leonard F. Register, Allan H. MacDonald and Sanjay K. Banerjee, "Effect of interlayer bare tunneling on electron-hole coherence in graphene bilayers," Physical Review B, *accepted for publication and in proof at time of writing*.

18. John. K. David, Leonard. F. Register and Sanjay K. Banerjee, "3D-Monte Carlo Study of Short Channel Trigate Nanowire MOSFETs," Solid-State Electronics **61**, 7-12. (July 2011).
19. (D. Basu, L. F. Register, A. H. MacDonald and S. K. Banerjee, "On the effect of interlayer bare tunneling on electron-hole condensates and critical interlayer currents in two coupled graphene layers" Physical Review B, in review.)
20. Dharmendar Reddy, Leonard F. Register, Gary D. Carpenter, Sanjay K. Banerjee," Graphene Field-effect Transistors," Journal of Physics D: Applied Physics, J. Phys. D: Appl. Phys. 44 (2011) 313001. (**Invited** journal paper).
21. Se-Hoon Lee, Aneesh Nainani, Jungwoo Oh, Kanghoon Jeon, Paul D. Kirsch, Prashant Majhi, Leonard Franklin Register, Sanjay K. Banerjee, and Raj Jammy, " ON-State Performance Enhancement and Channel-Direction-Dependent Performance of a Biaxial Compressive Strained Si0.5Ge0.5 Quantum-Well pMOSFET Along <110>and <100> Channel Directions," IEEE Electron Devices **58**, 985-995. (2011).
22. Leonard F. Register, M. M. Hasan, and Sanjay. K. Banerjee, "Stepped Broken-Gap Heterobarrier Tunneling Field-Effect Transistor for Ultralow Power and High Speed," IEEE Electron Device Lett. **32**, 743-745 (June 2011).
23. Jiwon Chang, Leonard F. Register, Sanjay K. Banerjee, and Bhagawan Sahu, "Density functional study of ternary topological insulator thin films", Phys. Rev. B **83**, article No. 235108 (2011).
24. Keng-Ming Liu, Leonard F. Register, and Sanjay K. Banerjee, "Quantum Transport Simulation of Strain and Orientation Effect in Sub-20nm Silicon-on-Insulator FinFETs," IEEE Transactions on Electron Devices 58,.4-10, (Jan 2011).
25. S. K. Banjerjee, L.F.Register, E. Tutuc, D.Basu, S.Kim, D.Reddy and A.H. MacDonald, "Graphene for CMOS and Beyond CMOS Applications," S. K. Banerjee, L. F. Register, E. Tutuc, D. Basu, S. Kim, D. Reddy and A.H. MacDonald, Proceedings of IEEE **98**(12), 2032 (Dec. 2010). (**Invited journal paper**).
26. Dipanjan Basu, Leonard. F. Register, Dharmendar Reddy, A. H. MacDonald and S. K. Banerjee, "Tight-binding study of electron-hole pair condensation in graphene bilayers: Gate control and system-parameter dependence", Phys. Rev. B **82**, article number 075409 (2010). DOI: 10.1103/PhysRevB.82.075409. (2010)
27. Jiwon Chang, Leonard F. Register, Ashok K. Kapoor and Sanjay K. Banerjee, "Analytical Model of Short-Channel Double-Gate JFETs," IEEE Transaction on Electron Devices **57**, 1846-1855 (2010).
28. Dharmendar Reddy, Leonard F. Register, Emanuel Tutuc, and Sanjay K. Banerjee, "Bilayer Pseudospin Field Effect Transistor: Applications to Boolean logic," IEEE Transactions on Electron Devices **57**, 755-764 (2010).
29. R. J. Zaman, K. Mathews, M. M. Hasan, W. Xiong, L. F. Register, and S. K. Banerjee, "A Novel Low Cost Tri-gate Process Suitable for Embedded CMOS 1T-1C Pseudo-SRAM Application," IEEE Transaction on Electron Device **56**, 448-455 (March 2009).
30. S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy and A. H. MacDonald, "Bilayer pseudoSpin Field-Effect Transistor (BiSFET): A proposed new logic device, IEEE Electron Device Letters **30**, 158-160, (February, 2009).
31. K.-M. Liu, W. Chen, L. F. Register and S. K. Banerjee, "Schrödinger equation Monte Carlo in three dimensions for simulation of carrier transport in three-dimensional nanoscale metal oxide semiconductor field-effect transistors," Journal of Applied Physics **104**, article number 114515 (Dec, 2008).
32. W.-Q. Chen, L. F. Register and S. K. Banerjee, "Schrodinger equation Monte Carlo in two dimensions for simulation of nanoscale metal-oxide-semiconductor field effect transistors," Journal of Applied Physics **103**, article number 024508 (January 15, 2008).
33. D. Basu, M. J. Gilbert, L. F. Register, S. K. Banerjee and A. H. Macdonald, "Effect of edge roughness on electronic transport in graphene nanoribbon channel metal-oxide-semiconductor field-effect transistors," Applied Physics Letters **92,** article number 042114 (JAN 28 2008).

34. X.-F. Fan, L. F. Register, B. Winstead M. Foisy, W Chen. X. Zheng, B. Ghosh, and S. K. Banerjee, "Hole Mobility and Thermal Velocity Enhancement for Uniaxial Stress in Si up to 4 GPa," IEEE Transactions on Electron Devices **54**, no.2, pp. 291-296 (February 2007).
35. F. Li., L. F. Register, M. M. Hasan, and S. K. Banerjee, "A program for Device Model Parameter Extraction for Gate Capacitance and Current of Ultrathin SiO_2 and High-K Gate Stacks," IEEE Transactions on Electron Devices **53**, 2118-2127 (2006) (**Invited** journal paper).
36. X. Zheng, W. Chen, M. Stroscio and L. F. Register, "Nonequilibrium Green's function analysis of interwell transport and scattering in monopolar lasers," Physical Review B **73**, article number 245304 (2006).
37. S. Ganguly, A. H. MacDonald, L. F. Register and S. Banjerjee, "Intrinsic Curie temperature bistability in Ferromagnetic semiconductor resonant tunneling diodes," Physical Review B **73**, article number 033310 (2006).
38. S. Ganguly, Leonard F. Register, Allan H. MacDonald, And Sanjay K. Banerjee, "Two-Level Voltage Controlled Magnetization Switch Using a Ferromagnetic Semiconductor Resonant-Tunneling Diode," IEEE Transaction of Nanotechnology **5**, 30-33 (October 2006).
39. B. Ghosh, Xiao-Feng Fan, L. F. Register and S.K. Banerjee, "Monte Carlo study of strained germanium nanoscale bulk pMOSFETs," IEEE Transactions on Electron Devices **53**, 533-537, (March 2006).
40. F. Li., S. P. Mudanai, H.-H. Tseng, L. F. Register, P. J. Tobin, and S. K. Banerjee, "Asymmetry in Gate Capacitance-Voltage (C-V) Behavior of Ultrathin Metal Gate MOSFETs with HfO_2 Gate Dielectrics," IEEE Transactions on Electron Devices **53**, 1943-1946 (2006).
41. B. Ghosh, Jer-Hueih Chen, Xiao-Feng Fan, L.F. Register and S.K. Banerjee, "Monte Carlo study of remote Coulomb and remote surface roughness scattering in nanoscale Ge PMOSFETs with ultrathin high-κ dielectrics Preview," Solid-State Electronics **50**, 248-253, (Feb. 2006).
42. F. Li. S. P. Mudanai, Y.-Y. Fan, L. F. Register and S. K. Banerjee, "A physically-based quantum mechanical compact model of MOS device substrate-injected tunneling current through ultra-thin (EOT ~1nm) SiO_2 and high-k gate stacks," IEEE transactions on Electron Devices **53**, 1096-1106 (2006).
43. Tongsheng Xia, Leonard F. Register, and Sanjay K. Banerjee, "Transmission through the band gap states in Schottky barrier carbon nanotube transistors," IEEE Transactions on Nanotechnology **5**, 80-83, (MARCH 2006).
44. Tongsheng Xia, Leonard F. Register, and Sanjay K. Banerjee, "Simulation study of the carbon nanotube field effect transistors beyond the complex band structure region", Solid-State Electronics **49**, 860-864, (May, 2005).
45. F. Li, S. P. Mudanai, L. F. Register, S. K. Banerjee, "A Physically Based Compact Gate *C-V* Model for Ultrathin (EOT ~ 1 nm and below) Gate Dielectric MOS Devices," IEEE Trans. Electron Devices **52**, 1148-1158, 2005.
46. B. Ghosh, X. Wang, X. F. Fan, L. F. Register, and S. K. Banerjee "Monte Carlo Study of Germanium n- and pMOSFETs," IEEE Transactions on Electron Devices **52**, 547-553 (April 2005).
47. Swaroop Ganguly, L. F. Register, S. Banerjee, and A. H. MacDonald, "Bias Voltage Controlled Magnetization Switch in Ferromagnetic Semiconductor Resonant Tunneling Diodes," Phys. Rev. B **71**, article number 245306 (2005).
48. T.-S. Xia, L. F. Register, and S. K. Banerjee, "Calculations and applications of the Complex band structure for carbon nanotube field-effect transistors," Phys. Rev. B. **70**, 45322 (2004).
49. Xiao-Feng Fan, Xin Wang, Brian Winstead, Leonard F. Register, Umberto Ravaioli, and Sanjay K. Banerjee, "Monte Carlo simulation of strained Si MOSFET with full-band structure and quantum correc**ti**on," IEEE Trans. Electron Devices **51**, 962-970 (2004).
50. T.-S. Xia, L. F. Register, and S. K. Banerjee, "Quantum transport in carbon nanotube transistors: Complex band structure effects" J. Appl. Phys. **95**, 1597 (2004).

51. Y. Y. Fan, Q Xiang, J. An, L. F. Register and S. K. Banerjee, “Impact of Interfacial Layer Transistion Region on Gate Current Performance for High-k Gate Dielectric Stack: Its Tradeoff with Gate Capacitance,” IEEE Transaction on Electron Devices **50**, 433-439 (2003).
52. T.-S. Xia, L. F. Register and S. K. Banerjee, “Quantum Transport in Double-Gate MOSFETs with Complex Bandstructure,” IEEE Trans. Electron Devices **50**, 1511-1516 (2003).
53. Y.-Y. Fan, R. Nieh, J. Lee, G. Lucovsky, G. Brown , L. F. Register and S. K. Banerjee, “Voltage and Temperature Dependent Gate Capacitance and Current Model: Application to ZrO_2 n-Channel MOS Capacitor,” IEEE Trans. Electron. Devices **49**, 1969-1978 (2003).
54. X. Wang, D. L. Kencke, K. C. Liu, L. F. Register, S. K. Banerjee, et al., “Band Alignments in Side-Wall Strained Si/Strained SiGe Heterostructures,” Solid State Electron Devices **46**, 2021-2025 (Dec. 2002).
55. S. P. Mudanai, F. Li, S. B. Samavedam, L. F. Register, S. K. Banerjee et al. “Interfacial Defect States in HfO_2 and ZrO_2 Capacitors,” IEEE Electron Devices Letters **23**, 728-730 (Dec. 2002).
56. W. Chen, L. F. Register and S. K. Banerjee, “Simulation of Quantum Effects Along the Channel of Ultrascaled Si-Based MOSFETs,” IEEE Trans. on Electron Devices **49** pp.652-657 (April 2002).
57. S. Mudanai, L. F. Register, A. F. Tasch, and S. K. Banerjee, "Understanding the effects of Wave Function Penetration on the Inversion Layer Capacitance of NMOSFETs," IEEE Electron Device Letters **22,** 145 (2001).
58. Q. Ouyang, X. D. Chen, A. F. Tasch, L. F. Register, and S. K. Banerjee, "Built-in Logitudinal Field Effects in Sub-100 nm Graded $Si_{1-x}Ge_x$ Channel P-MOSFETS," IEEE Trans. on Electron Devices **48**, 1245-1250 (2001).
59. Xin Wang, D. L. Kencke, K. C. Liu, A. F. Tasch, Jr., L. F. Register, and S. K. Banerjee, "Monte Carlo Simulation on Electron Transport in simple Orthorhombically-strained Silicon", J. Appl. Phys. **88**, 4717 (2000).
60. Q. Ouyang, Xi. Chen, S. Mudanai, X. Wang, D. L. Kencke. A. F. Tasch. L. F. Register, and S. K. Banerjee, "A Novel Si/SiGe Heterojunction pMOSFET with reduced Short-Channel Effects and Enhanced Drive Current," IEEE Transactions on Electron Devices **47**, (2000).
61. L. F. Register and K. Hess, “Improved Algorithm for Modeling Collision Broadening Through a Sequence of Scattering Events,” *Journal of Applied Physics* **87**, 303-311 (2000).
62. K. Hess, B. Tuttle, L. F. Register and D. K. Ferry, “Magnitude of the Threshold Energy for Hot Electron Damage in MOSFETs by Hydrogen Desorption,” *Appl. Phys. Lett.*, 75, pp. 3147-3149 (1999).
63. L. F. Register, E. Rosenbaum and K. Yang, “Analytic Model for Direct Tunneling in Poly-Gate Metal-Oxide-Semiconductor Devices,” *Applied Physics Letters* **74**, 457-459 (1999).
64. B. Klein, L. F. Register, K. Hess, D. G. Deppe and Q. Deng, “Self-consistent Green’s Function Approach to the Analysis of Dielectrically-apertured Vertical-cavity Surface-emitting Lasers,” *Appl. Phys. Lett.,* **73**, (23), pp. 3324-3326 (1998).
65. B. Klein, L. F. Register, M. Grupen and K. Hess, "Numerical Simulation of Vertical Cavity Surface Emitting Lasers," *Optics Express,* **2** (4), pp. 163-168 (1998) (http://epubs.osa.org/opticsexpress/)
66. L. F. Register and K. Hess, "Simulation of Carrier Capture in Semiconductor Quantum Wells: Bridging the Gap from Quantum to Classical Transport," *Appl. Phys. Letts*, **71**, 1222-1224, September, (1997).
67. E. Rosenbaum and L. F. Register, “Mechanism of Stress-Induced Leakage Current in MOS Capacitors,” IEEE Transactions on Electron Devices **44**, 317-323 (1997).
68. L. F. Register, R. Baca, G. Kosinovsky, M. Grupen and K. Hess, "Possibility of Off-Resonance Lasing in Vertical Cavity Surface Emitting Lasers," *Appl. Phys. Lett.,* **66**, (3), pp. 259-261. (1995)
69. D. V. Averin, L. F. Register, K. K. Likharev and K. Hess, "Single-Electron Coulomb Exclusion on the Atomic Level," *Applied Physics Letters*, **64** (1), pp. 126-128 (1994).
70. L. Register and K. Hess, "Numerical Simulation of Electron Transport in Mesoscopic Structures with Weak Dissipation," *Phys. Rev. B*, **49** (3), pp. 1900-1907, (1994).
71. Leonard F. Register, “Microscopic Basis for a Sum Rule for Polar-Optical-Phonon Scattering of Carriers in Heterostructures,” Physical Review B **45**, 8756-8759 (1992).

72. Leonard F. Register, Umberto Ravaioli, and Karl Hess, "Numerical Simulation of Mesoscopic Systems With Open Boundaries Using The Multidimensional Time-Dependent Schrödinger Equation," *J. Appl. Phys*. **69** (10), pp. 7153-7158 (1991).
73. Leonard F. Register, M. A. Stroscio, and M. A. Littlejohn, "Constraints on the Polar-Optical-Phonon Influence Functional in Heterostructures," Physical Review B **44**, 3850-3853 (1991).

REFEREED CONFERENCE PROCEEDINGS (20 in rank as Associate Professor)[12]

74. Jiwon Chang, Leonard F. Register, Sanjay K. Banerjee, and Bhagawan Sahu, "Effect of Dielectric Materials on the Topological Insulator Bi2Se3 Surface States," Techcon 2011, Austin, TX, September 12-13, accepted.
75. Mohammad M. Hasan, Leonard F. Register and Sanjay K. Banerjee, "Stepped broken-gap Hetero-barrier Tunnel Field Effect Transistor (HetTFET) for ultra-low power and high speed," Techcon 2010, Austin, TX, September 13-14.
76. L. F. Register, Dipanjan Basu, Mohammad M. Hasan, Dharmendar Reddy and Sanjay K. Banerjee, "Changing Front-End Dielectric Requirement for End-of-the-Roadmap CMOS and Beyond," presented at 2010 Electrochemcial Society Meeting, Vancouver, Ca, April 26-30th, ECS Transactions 28, 3-17 (2010) 10.1149/1.3372560 (**Invited**).
77. D. Basu, L.F. Register, A. H. MacDonald and S. K. Banerjee, "Interlayer Tunneling Across Coupled Graphene Nanoribbons," TechCon 2009 (Austin, Texas, September 14th-15th, 2009).
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OTHER SIGNIFICANT PRESENTATIONS AND PUBLICATIONS:

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147. Leonard F. Register, Dipanjan Basu, Priyamvada Jadaun, Xuehao Mau, Dharmendar Reddy, Allan McDonald, Garry Carpenter, Sanjay Banerjee, "Graphene Nanoelectronics Beyond Current Technologies: a Simulation Perspective," NanoTech, Boston, MA, June 13-16, 2011. (**Invited presentation**)
148. Leonard. F. Register, "Multiscale Modeling of the Bilayer pseudo-spin Field effect transistor (BiSGET), a possible beyond CMOS graphene-based device," Army Research Laboratory workshop on Multi-Scale Multi-Disciplinary Modeling of Electronic Materials, September 1-2, 2010. (**Invited presentation**.)

149. S.K. Banerjee, L.F. Register, E. Tutuc, D. Akinwande, L. Colombo and G. Carpenter, "Graphene Nanoelectronics," NanoTech, Boston, MA, June 13-16, 2011. (**Invited presentation**)
150. S. Banerjee, E. Tutuc and L.F.Register, "Characterization and Modeling of Exfoliated and CVD Graphene Field Effect Transistors," GOMAC 2010. (**Invited presentation**)
151. Sanjay Banerjee, L.Register, E.Tutuc, R.Ruoff, A.MacDonald, L.Colombo*, G.Carpenter#, S.Kim. D.Basu, D. Reddy, "Graphene FETs and Beyond, Sanjay Banerjee, L.Register, E.Tutuc, R.Ruoff, A.MacDonald, L.Colombo, G. Carpenter, S. Kim. D. Basu, D. Reddy, Carbon Electronics Workshop, Albany, NY, Sept. 2010. (**Invited presentation**)
152. S. Kim, E. Tutuc, R. Ruoff, L. F. Register, S. K. Banerjee, "Graphene for Beyond Scaled CMOS, Luigi Colombo," SEMATECH International Gate Stack Workshop, Sept.2010. (**Invited presentation**)
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154. Leonard F. Register, "The Bilayer Puedospin Field Effect Transistor (BiSFET); a proposed new logic device," **Invited** keynote talk to TechCon 2009 (Austin, Texas, September 14th-15th, 2009).
155. Dharmendar Reddy, Leonard F. Register, Emanuel Tutuc, Gary D. Carpenter, Allan MacDonald, and Sanjay K. Banerjee, "Bilayer pseudoSpin Field Effect Transistor for Beyond CMOS Logic," INC6 Grenoble, France (May, 2010).
156. S. Banerjee, F. Register, E. Tutuc, A. Macdonald, "BiSFET- A Proposed new Logic Switch," **Invited** talk*, Frontiers of Electronics Symposium, Harvard,* May 30, 2009.
157. S. K. Banerjee, L. F. Register, E. Tutuc, A. Macdonald, D. Reddy and D. Basu, "Microelectronics: the Beginning of the end or the end of the beginning?", **Invited** Keynote, ACM TAU workshop, Austin, TX, Feb. 2009.
158. L. F. Register, "Essential Transport Physics of Nanoscale MOSFETs," CMOS Emerging Technologies Workshop, Banff, Canada, February 17-20, 2009 (**Invited** talk).
159. L. F. Register, "Nanoscale MOSFET physics: observations from non-compact modeling studies," Frontiers in Compact Modeling Workshop, California, October, 2008 (**Invited** talk).
160. D. Basu, M. J. Gilbert, L. F. Register, and S. K. Banerjee, "Effects of Non-Ideal Edges in Graphene Nanoribbons," APS March Meeting 2008, New Orleans, August 2008.
161. L. F. Register and Banerjee (presenters) "Southwest Academy of Nanotechnology (SWAN)," 4th International Nanotechnology Conference (INC4), April 14-17, 2008, Tokyo, Japan (**Invited** poster).
162. L. F. Register (presenting author) "Resonant-injection-augmented Field Effect Transistor (RIAFET) for low voltage switching, 4th International Nanotechnology Conference (INC4), April 14-17, 2008 Tokyo, Japan (**Invited** poster).
163. L. F. Register, "Modeling and simulation issues and approaches for ultimate CMOS and beyond," IEEE Electron Devices Council, central Texas chapter (at Sematech) **Invited** talk, July 2007
164. Leonard F. Register, Wanqiang Chen, and Sanjay K. Banerjee, "Schrödinger Equation Monte Carlo-2D for simulation of quantum transport and scattering in nano-scale non-classical CMOS", 5th Motorola Workshop on Computational Materials and Electronics (MWCME) 11/14-15/2003 (**Invited** talk).
165. L. F. Register, W. Chen, "Phonon Scattering in Nanostructures: Function and Challenges to Modeling," *IEEE NANO 2002*, Arlington, VA, Aug. 26-28, 2002. **(Invited** talk).
166. Leonard F. Register, "Gate Current and Capacitance Modeling," presentation to the Compact Modeling Council, Dallas Texas, March, 2001 (**Invited** talk).