EARL E. SWARTZLANDER, JR.
Professor of Electrical and Computer Engineering
University of Texas at Austin
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EDUCATION:

Ph.D.	University of Southern California	Los Angeles, CA	June, 1972
M.S.E.E.	University of Colorado	Boulder, CO	June, 1969
B.S.E.E.	Purdue University	West Lafayette, IN	January, 1967

CURRENT POSITION:

Professor September 2006 to Present
Professor/Schlumberger Centennial Chair in Engineering 1990 to 2006
University of Texas/Department of Electrical and Computer Engineering
Conducting research in computer engineering with emphasis on application specific processor design, including special purpose computer architecture, high-speed computer arithmetic, signal processor architecture, VLSI technology, and nanotechnology. Currently teaching courses in circuit analysis and high-speed computer arithmetic.

PREVIOUS POSITIONS:

Director of Independent Research & Development 1987 to 1990
TRW/Defense Systems Group
Responsible for defining, directing, and managing the Independent Research & Development program for the Defense Systems Group of TRW. Identified the needs, developed projects, and monitored the progress of a $20 M per year IRAD Program.

Manager, Digital Processing Laboratory 1985 to 1987
TRW/Electronics & Technology Division, Redondo Beach, CA
Managed a laboratory of 150 people who develop advanced digital systems (A/D Converters, Signal Processors, and Distributed Computing Systems.) This involved personnel and technical leadership in a broad range of technologies including analog to digital converters, custom and semi-custom VLSI development, silicon compilers, signal processing, and special purpose processors (i.e., architecture, design, and implementation.)

Manager, Advanced Development Office 1982 to 1985
TRW/System Development Division, Redondo Beach, CA
Led the development of the Modular Transform Processor, a 40 MSPS FFT processor, involving collaboration between TRW and AT&T Technologies that produced the first semi-custom VLSI circuit with over 100,000 transistors. This project successfully introduced advanced hardware technology into a software/systems engineering organization in TRW. Also led a multi-division

project that developed the TRW LSI Products TMC 2301 commercial Image Resampling Sequencer VLSI circuit for real time video image manipulation.

Assistant Manager, Huntsville Laboratory 1980 to 1982
TRW/Systems Engineering and Integration Division, Huntsville, AL
Managed systems development and methodology research in decentralized and distributed data processing for ballistic missile defense radar signal processing applications. Performed a study of VLSI implementation to improve frequency domain adaptive digital filters.

Staff Engineer and Senior Staff Engineer 1975 to 1980
TRW/Digital Development Laboratory, Redondo Beach, CA
Technical contributor and manager of studies and small projects in VLSI architecture and application, signal processor hardware development for sonar and avionics applications, computer networking, and radar digital beam forming.

Chief Engineer 1974 to 1975
Geophysical Systems Corp., Pasadena, CA
Responsible for field support of a geophysical data acquisition/data reduction system for field processing of seismic data.

Member of the Research Staff 1973 to 1974
Technology Service Corp., Santa Monica, CA.
Managed the development, checkout, production and initial field support of a security monitoring system.

Hughes Doctoral Fellow and Staff Engineer 1969 to 1973
Hughes Aircraft Co., Culver City, CA
Developed special purpose display systems for avionics human factor research, designed novel arithmetic algorithms, and provided technical support to CODEM, a project for full wafer LSI implementation of a spread spectrum avionics communication system.

Development Engineer 1967 to 1969
Ball Brothers Research Corp., Boulder, CO
Designed and supervised the fabrication and check-out of the electronics and data handling system of the Harvard College Observatory Spectroheliometer for the Apollo Telescope Mount ("flown," on Skylab).

HONORS AND AWARDS:
IEEE Third Millennium Medal from IEEE Solid-State Circuits Society, 2000

University of Colorado Distinguished Engineering Alumnus Award, 1997

Awards for service to the IEEE Wafer Scale Integration and IEEE Innovative Systems in Silicon conferences, 1997

Inaugural member of the Golden Core of the IEEE Computer Society, 1996

Knight, Imperial Russian Order of Saint John of Jerusalem (Knights of Malta), 1993

Purdue University Outstanding Electrical Engineer, 1992

Schlumberger Centennial Chair in Engineering, 1990 to 2006

TRW Defense Systems Group Chairman's Award for Innovation, 1989

Purdue University Distinguished Engineering Alumnus, 1989

Fellow of the IEEE for contributions to VLSI design of specialized signal processors, 1988

TRW Independent Research and Development Roll of Honor, 1984

Howard Hughes Doctoral Fellow, 1969 to 1972

Six Technical paper awards

Six Meritorious Service Awards and Certificates of Appreciation from the IEEE Computer Society

Who's Who Listings:
Who's Who in America
Who's Who in American Education
Who's Who in Finance and Industry
Who's Who in the South and Southwest
Who's Who in Science and Engineering
Who's Who in the World

JOURNALS EDITED:

Hardware Area Editor: *ACM Computing Reviews,* 1985 to present
History of Computing Area Editor: *ACM Computing Reviews,* 2012 to present
Computer Arithmetic and DSP Architecture Editor: *Journal of Systems Architecture,* 1994 to 2006
Editor of "Calculators" Column, *IEEE Annals of the History of Computing*, 1995 to 2001
Editor-in-Chief: *IEEE Transactions on Signal Processing*, 1995
Editor-in-Chief: *IEEE Transactions on Computers*, 1991 to 1994
Editor-in-Chief: *Journal of VLSI Signal Processing*, 1989 to 1995
Associate Editor: *IEEE Transactions on Parallel and Distributed Systems*, 1989 to 1991
Associate Editor: *IEEE Journal of Solid-State Circuits,* 1984 to 1988
Editorial Board: *Journal of Signal Processing Systems for Signal, Image, and Video Technology,* 1996 to present
Editorial Board: *Journal of Parallel and Distributed Computing,* 1983 to 1986
Editor: *IEEE Transactions on Computers,* 1982 to 1986
Advisory Board: *Journal of Microelectronic System Integration,* 1993 to 2005
Editorial Advisory Board: *VLSI Design,* 1993 to present
Editorial Board: Wiley *Encyclopedia of Electrical and Electronics Engineering,* 1997 to 1998

TECHNICAL LEADERSHIP:

IEEE Awards Board
Member-at-large, 2015 to 2016

IEEE Awards Board Awards Review Committee
Chair 2015 to 2016
Member-at-large, 2014

IEEE Awards Planning and Policy Committee

Vice Chair 2012 to 2013
Member-at-large, 2011 to 2013

IEEE James H. Mulligan, Jr. Education Medal Committee
Past-Chair, 2011
Chair, 2009 to 2010
Member, 2006 to 2008

IEEE Fellows Committee
Member, 2000 to 2003

IEEE History Committee
Member, 1996 to 2004
Chair IEEE History Fellowship Sub-Committee, 1998 to 2004

IEEE Signal Processing Society
ADCOM/Board of Governors, 1992 to 1994

IEEE Solid-State Circuits Council/Society
Treasurer, 1994 to 1998
Secretary, 1992 to 1993
ADCOM (IEEE Computer Society representative), 1986 to 1991

IEEE Computer Society
Board of Governors, 1987 to 1991
Chair of the Technical Committee on Real-Time Systems, 1982 to 1983
Chair of the Technical Committee on Data Acquisition and Control, 1981

CONFERENCE ORGANIZATION AND LEADERSHIP:
General Chair or Co-General Chair:

2011 IEEE International Conference on Application-Specific Systems, Architectures, and Processors (Santa Monica, CA, September 2011)

2000 IEEE Workshop on Signal Processing Systems (SiPS) (Lafayette, LA, October 11-13, 2000)

2000 IEEE International Conference on Application-Specific Systems, Architectures, and Processors (Boston, MA, July 10-12, 2000)

31st Asilomar Conference on Signals, Systems & Computers (Monterey, CA, 1997)

1994 International Conference on Application Specific Array Processors (San Francisco)

1993 International Conference on Parallel and Distributed Systems, Taiwan

11th Symposium on Computer Arithmetic (Windsor, Canada, 1993)

1990 International Conference on Application Specific Array Processors (Princeton)

International Conference on Wafer Scale Integration (San Francisco, 1989)

5th IEEE International Conference on Distributed Computing Systems (Denver, 1985)

1982 IEEE Real-Time Systems Symposium (Los Angeles)

1981 IEEE Real-Time Systems Symposium (Miami)

IEEE Distributed Data Acquisition, Computing, and Control Symposium (Miami, 1980)

Program Chair or Co-Program Chair:

1999 Volta Workshop on Low Power Circuits and Systems, (Como, Italy, 1999)

30th Asilomar Conference on Signals, Systems & Computers (Monterey, 1996)

6th IEEE Symposium on Parallel and Distributed Processing (Dallas, 1994)

9th Symposium on Computer Arithmetic (Santa Monica, 1989)

1989 International Conference on Systolic Arrays (Killarney, Ireland)

1988 International Conference on Systolic Arrays (San Diego)

1986 International Conference on Parallel Processing (Chicago)

4th IEEE International Conference on Distributed Computing Systems (San Francisco, 1984)

Steering Committees:

IEEE Symposia on Computer Arithmetic, 2003 to present

Asilomar Conference on Signals, Systems and Computers, 1997 to present

IEEE Transactions on VLSI Systems, 1993 to 2000

Civic Leadership:

Benedict Hills Estates Homeowners Association (Beverly Hills, CA),
Board of Directors, 1984 to 2006
President, 1990 to 1995

Casiano Estates Homeowners Association (Bel Air, CA)
Board of Directors, 1976 to 1978
President, 1978 to 1980

PERSONAL:

Citizen of USA

Registered Professional Engineer in California, Colorado, and Texas

Member of Eta Kappa Nu, Sigma Tau, and Omicron Delta Kappa honorary fraternities

PATENTS:

Issued (16):

Jongwook Sohn and Earl E. Swartzlander, Jr., "Improved Fused Floating-Point Add-Subtract Unit," US patent no. 9,317,478, Issued April 19, 2016.

Earl E. Swartzlander, Jr. and Jongwook Sohn, "Dual-Path Fused Floating-Point Two-Term Dot product Unit," US patent no. 8,626,813, Issued January 7, 2014.

Moises E. Robinson, Marwan M. Hassoun and Earl E. Swartzlander, Jr., "Method and Apparatus for Capacitance Multiplication Within a Phase Locked Loop," Canada Patent no. 2,632,006, issued July 16, 2013.

Earl E. Swartzlander, Jr. and Inwook Kong, "Data Tag Control Method for Quantum-dot Cellular Automata," U.S. patent no. 8,415,968, issued April 9, 2013.

Earl E. Swartzlander, Jr. and Inwook Kong, "Machine Division," U.S. patent no. 8,407,274, issued March 26, 2013.

Moises E. Robinson, Marwan M. Hassoun and Earl E. Swartzlander, Jr., "Method and Apparatus for Capacitance Multiplication Within a Phase Locked Loop," China patent no. 101,326,721, filed December 6, 2006, Issued March 6, 2013, OTC-5391-SWA.

Earl E. Swartzlander, Jr. and Hani H. Saleh, "Floating-Point Fused Dot-Product Unit," U.S. patent no. 8,166,091, issued April 24, 2012.

Earl E. Swartzlander, Jr. and Hani Saleh, "Fused Floating-Point Add Subtract Unit," U.S. patent no. 8,161,090, issued April 17, 2012.

Moises E. Robinson, Marwan M. Hassoun and Earl E. Swartzlander, Jr., "Method and Device for Capacitance Multiplication Inside Phase Locked Loop," Japan patent no. 4,856,191, filed December 5, 2006, Issued January 18, 2012, OTC-5391-SWA.

Earl E. Swartzlander, Jr., "Negative Two's Complement Processor for Windowing in Harmonic Analysis," U.S. patent no. 8,099,447, issued January 17, 2012.

Eric Quinnell, Earl E. Swartzlander, Jr., and Carl Lemonds, "Bridge Fused Multiply-Adder Circuit," U.S. patent no. 8,078,660, issued December 13, 2011.

Eric Quinnell, Earl E. Swartzlander, Jr., and Carl Lemonds, "Three-Path Fused Multiply-Adder Circuit," U.S. patent no. 8,037,118, issued October 11, 2011.

Giri N. K. Rangan and Earl E. Swartzlander, Jr., "Voltage Controlled Oscillator," U.S. patent no. 7,737,795, issued June 15, 2010.

Earl E. Swartzlander, Jr. and Ayman M. El-Khashab, "Modular Pipeline Fast Fourier Transform," U.S. Patent no. 7,543,010, issued June 2, 2009.

Moises E. Robinson, Shahriar Rokhsaz, Marwan M. Hassoun and Earl E. Swartzlander, Jr., "Voltage Controlled Oscillator," U.S. Patent no. 7,315,220, issued January 1, 2008.

Moises E. Robinson, Marwan M. Hassoun and Earl E. Swartzlander, Jr., "Method and Apparatus for Capacitance Multiplication Within a Phase Locked Loop," U.S. Patent no. 7,307,460, issued December 11, 2007.

PUBLICATIONS:

Books (2):

Weiqiang Liu, Earl E. Swartzlander, Jr. and Máire O'Neill, *Design of Semiconductor QCA Systems*, Boston: Artech House, 2013.

Earl E. Swartzlander, Jr., *VLSI Signal Processing Systems*, Boston: Kluwer Academic Publishers, 1986.

Edited Books (11):

Earl E. Swartzlander, Jr., ed., *Computer Arithmetic*, Volume I, Singapore: World Scientific Publishing, 2015.

Earl E. Swartzlander, Jr., ed., *Computer Arithmetic*, Volume II, Singapore: World Scientific Publishing, 2015.

Earl E. Swartzlander, Jr. and Carl Lemonds, Jr., eds., *Computer Arithmetic*, Volume III,

Singapore: World Scientific Publishing, 2015.

Earl E. Swartzlander, Jr., *Application Specific Processors*, Boston: Kluwer Academic Publishers, 1997.

M. A. Bayoumi and Earl E. Swartzlander, Jr., *VLSI Signal Processing Technology*, Boston: Kluwer Academic Publishers, 1994.

Earl E. Swartzlander, Jr., *Computer Arithmetic*, Vol. 2, Los Alamitos, CA: IEEE Computer Society Press, 1990.

Earl E. Swartzlander, Jr., *Computer Arithmetic*, Vol. 1, Los Alamitos, CA: IEEE Computer Society Press, 1990.

Earl E. Swartzlander, Jr., *Wafer Scale Integration*, Boston: Kluwer Academic Publishers, 1989.

Earl E. Swartzlander, Jr., *Systolic Signal Processing Systems*, New York: Marcel Dekker, Inc., 1987.

Earl E. Swartzlander, Jr., *Computer Arithmetic*, Stroudsburg, PA: Dowden, Hutchinson & Ross, Inc., 1980, second edition Los Alamitos, CA: IEEE Computer Society Press, 1990.

Earl E. Swartzlander, Jr., *Computer Design Development: Principal Papers*, Rochelle Park, NJ: Hayden Book Co., 1976.

Book Chapters (40):

Earl E. Swartzlander Jr., Heumpil Cho, Inwook Kong, and Seong-Wan Kim, "Arithmetic Implemented with Semiconductor Quantum-Dot Cellular Automata," in Tomasz Wojcicki, ed., VLSI Circuits for Emerging Applications, Boca Raton, FL: CRC Press, 2014, pp. 16-48.

Weiqiang Liu, Saket Srivastava, Máire O'Neill, and Earl E. Swartzlander, Jr., "Security Issues in QCA Circuit Design - Power Analysis Attacks," in Neal Anderson and Sanjukta Bhanja, eds., Field-Coupled Nanocomputing, *Lecture Notes in Computer Science*, vol. 8280, New York: Springer, 2014, pp. 194-222.

Earl E. Swartzlander, Jr. "High-Speed Computer Arithmetic," Ch. 20 in A. B. Tucker, Jr., ed., *Computing Handbook: Computer Science and Software Engineering*, vol. 1, 3rd Ed., Boca Raton, FL: CRC Press, 2014, pp. 20-1-20-28.

K'Andrea Bickerstaff and Earl E. Swartzlander, Jr., "Memristor-Based Addition and Multiplication," Andrew Adamatzky and Leon Chua, editors., *Memristor Networks*, London: Springer International Publishing, pp. 473-486, 2014.

Seong-Wan Kim and Earl E. Swartzlander, Jr. "Restoring Divider Design for Quantum-Dot Cellular Automata," James E. Morris and Kris Iniewski, editors, *Nanoelectronic Device Applications Handbook*, Boca Raton, FL: CRC Press, 2013, pp. 239-254.

Earl E. Swartzlander, Jr., "High-Speed Computer Arithmetic," Chapter 22 in Vojin Oklobdzija, editor, *The Computer Science and Engineering Handbook*, 3rd Ed., vol. 1, Boca Raton, FL: CRC Press, 2012, pp. 22-1-22-22.

Eric Quinnell and Earl E. Swartzlander, Jr., "Floating-Point Computer Arithmetic," Benjamin W. Wah, editor, *Wiley Encyclopedia of Computer Science and Engineering*, Hoboken: John Wiley and Sons, Inc., 2009, pp. 1275-1285.

Earl E. Swartzlander, Jr. "Fixed-Point Computer Arithmetic," Benjamin W. Wah, editor, *Wiley Encyclopedia of Computer Science and Engineering*, Hoboken: John Wiley and Sons, Inc., 2009, pp. 1264-1275.

Bassam Mohd, Earl E. Swartzlander, Jr. and Adnan Aziz, "The Hazard-Free Superscalar Pipeline Fast Fourier Transform Architecture and Algorithm," Ricardo Reis, Vincent Mooney and Paul Hasler, editors, *VLSI-SOC: Advanced Topics on Systems on a Chip*, IFIP vol. 291, Boston: Springer, 2009, pp. 227-248.

Earl E. Swartzlander, Jr. and Gensuke Goto, "Computer Arithmetic," Chapter 11 in Vojin Oklobdzija, editor, *Digital Design and Fabrication, The Computer Engineering Handbook*, 2nd Ed., Boca Raton, FL: CRC Press, 2008, pp. 11-1-11-38.

Earl E. Swartzlander, Jr., "Computer Arithmetic for VLSI Signal Processing," Chapter 80 in Wai-Kai Chen editor, *The VLSI Handbook*, 2nd Ed., Boca Raton, FL: CRC Press Taylor & Francis Group, 2007, pp. 80-5-80-28.

Earl E. Swartzlander, Jr., "High-Speed Computer Arithmetic," Chapter 22 in A. B. Tucker, Jr., editor, *Computer Science Handbook*, 2nd Ed., Boca Raton, FL: Chapman and Hall/CRC Press, 2004, pp. 22-1-22-22.

Earl E. Swartzlander, Jr., "Calculating Machines," in Atsushi Akera and Frederik Nebeker, editors, *From 0 to 1: An Authoritative History of Modern Computing*, New York: Oxford University Press, 2002. pp. 51-62.

Earl E. Swartzlander, Jr., "Baldwin-Odhner Calculators," "Leibniz Calculator," "Pascal Calculator" and "Slide Rule," Entries in Raul Rojas, editor, *Encyclopedia of Computers and Computer History*, Chicago: Fitzroy Dearborn Publishers, 2001, pp. 715-716.

Earl E. Swartzlander, Jr., "High-Speed Computer Arithmetic," Chapter 9 in Vojin Oklobdzija, editor, *Computer Engineering Handbook*, Boca Raton, FL: CRC Press, 2001, pp. 9-1-9-21.

Thomas K. Callaway and Earl E. Swartzlander, Jr., "The Power Consumption of CMOS Adders and Multipliers," in A. Chandrakasan and R. Broderson, editors, *Low Power CMOS Design*, New York: IEEE Press, 1998, pp. 218-224.

Earl E. Swartzlander, Jr., "Elaborazione di un Sistema Dedicato, la Chiave al Calcolatori Nascosti," in M. Morelli, editor, *Il Calcolatore Nascosto*, Milano, Italy: Etas Libri, 1996, pp. 121-134.

Earl E. Swartzlander, Jr., "High-Speed Computer Arithmetic," Chapter 19 in A. B. Tucker, Jr., editor, *Computer Science and Engineering Handbook*, Boca Raton, FL: CRC Press, 1996, pp. 462-481.

Thomas K. Callaway and Earl E. Swartzlander, Jr., "Low Power Arithmetic Components," Chapter 7 in J. M. Rabaey and M. Pedram, editors, *Low Power Design Methodologies*, Boston: Kluwer Academic Publishers, 1996, pp. 161-200.

Michael J. Schulte and Earl E. Swartzlander, Jr., "A Processor for Accurate, Self-Validating Computing," in G. Aleford, A. Frommer and B. Lang, editors, *Mathematical Research*, vol. 90, Berlin: Akademie Verlag, 1996, pp. 25-31.

Michael J. Schulte and Earl E. Swartzlander, Jr., "A Coprocessor for Accurate and Reliable Computing," in G. Aleford and J. Herzberger, editors, *Mathematical Research*, vol. 89, Berlin: Akademie Verlag, 1996, pp. 217-223.

Michael J. Schulte and Earl E. Swartzlander, Jr., "Software and Hardware Techniques for Accurate, Self-Validating Arithmetic," Chapter 14 in R. B. Kearfott and V. Kreinovich, editors, *Applications of Interval Computations*, Boston: Kluwer Academic Publishers, 1996, pp. 381-404.

H. H. Yao and Earl E. Swartzlander, Jr., "Serial-Parallel Multipliers," J. G. Ackenhusen, editor, *Signal Processing Technology and Applications*, New York, IEEE Press, 1995, pp. 213-217.

D. M. Samani, J. Ellinger, Edward J. Powers and Earl E. Swartzlander, Jr., "Implementation of Several RLS Nonlinear Adaptive Algorithms Using a Commercial Floating Point Digital Signal Processor," J. G. Ackenhusen, editor, *Signal Processing Technology and Applications*, New York, IEEE Press, 1995, pp. 316-320.

Thomas A. Ziaja and Earl E. Swartzlander, Jr., "Boundary Scan in Board Manufacturing," Chapter in M. Abadir and T. Ambler, editors, *Economics of Electronic Design, Manufacture and Test*, Boston: Kluwer Academic Publishers, 1994, pp. 137-142.

Earl E. Swartzlander, Jr., "Computer Arithmetic," Chapter 4 in C. H. Chen, editor, *Computer Engineering Handbook*, New York: McGraw-Hill, 1992, pp. 4.1-4.20.

Earl E. Swartzlander, Jr., "Application Specific VLSI Processors," Chapter 14 in C. H. Chen, editor, *Computer Engineering Handbook*, New York: McGraw-Hill, 1992, pp. 14.1-14.31.

Earl E. Swartzlander, Jr., "Wafer Scale Integration for the Implementation of Artificial Neural Networks," in M. Sami and J. Calzadilla-Daguerre, editors, *Silicon Architectures for Neural Nets*, Elsevier Science Publishers, 1991, pp. 179-185.

Earl E. Swartzlander, Jr., "Arithmetic-Logic Unit," Section 9.5 in B. D. Tapley, editor, *Eshbach's Handbook of Engineering Fundamentals*, New York: John Wiley & Sons, 1990, pp. 9.68-9.81.

D. J. McBride and Earl E. Swartzlander, Jr., "Architecture: Interrupt Systems and System States," Section 9.2 in B. D. Tapley, editor, *Eshbach's Handbook of Engineering Fundamentals*, New York: John Wiley & Sons, 1990, pp. 9.21-9.24.

Earl E. Swartzlander, Jr., "On-Board Radar Signal Processors," Chapter 14 in L. Cantafio, editor, *Space Based Radar*, Norwood, MA: Artech House, Inc., 1989, pp. 531-565.

Earl E. Swartzlander, Jr., "VLSI Signal Processing Systems," Chapter 8 in C. H. Chen, editor, *Signal Processing Handbook*, New York: Marcel Dekker, Inc., 1988, pp. 221-256.

Earl E. Swartzlander, Jr., "Systolic FFT Processors," Chapter 2.4 in W. Moore, Andrew McCabe and Roddy Urquhart, editors, *Systolic Arrays*, Boston: Adam Hilger, 1987, pp. 133-140.

Earl E. Swartzlander, Jr. and George Hallnor, "Frequency-Domain Digital Filtering with VLSI," Chapter 19 in S. Y. Kung, H. J. Whitehouse and T. Kailath, editors, *VLSI and Modern Signal Processing*, Englewood Cliffs: Prentice-Hall, 1985, pp. 349-359.

Earl E. Swartzlander, Jr., "Designing with Microprocessors," Section 1.18 in S. S. L. Chang, editor, *Fundamentals Handbook of Electrical and Computer Engineering*, Vol. III, New York: John Wiley & Sons, 1983, pp. 183-200.

Earl E. Swartzlander, Jr., "Arithmetic-Logic Unit," Section 1.5 in S. S. L. Chang, editor, *Fundamentals Handbook of Electrical and Computer Engineering*, Vol. III, New York: John Wiley & Sons, 1983, pp. 44-58.

D. J. McBride and Earl E. Swartzlander, Jr., "Architecture: Interrupt Systems and System States," Section 1.2 in S. S. L. Chang, editor, *Fundamentals Handbook of Electrical and Computer Engineering*, Vol. III, New York: John Wiley & Sons, 1983, pp. 22-27.

Earl E. Swartzlander, Jr., "VLSI Architecture," Chapter 6 in D. F. Barbe, editor, *VLSI Fundamentals and Applications*, New York: Springer-Verlag, 1980, pp. 178-221.

Earl E. Swartzlander, Jr., "Microprogrammed Sequential Networks," in *New Components and Subsystems for Digital Design*, Santa Monica, CA: Technology Service Corp., 1975, pp. 111-114.

Earl E. Swartzlander, Jr., "Computers for Pattern Recognition," in J. Rose, editor, *Advances in Cybernetics and Systems*, Vol. 1, New York: Gordon and Breach Science Publishers, 1974, pp. 389-396.

Refereed Journal Papers (84):

Lauren Guckert and Earl E. Swartzlander, Jr., "MAD Gates - Memristor Logic Design Using Driver Circuitry," *IEEE Transactions on Circuits and Systems-II*, TCAS-II-00173-2016, accepted April 3, 2016.

Xiaoping Cui, Weiqiang Liu, Xin Chen, Earl E. Swartzlander, Jr., and Fabrizio Lombardi, "A New Modified Partial Product Generator for Redundant Binary Multipliers," *IEEE Transactions on Computers*, vol. 65, April 2016, pp. 1165-1171.

Jongwook Sohn and Earl E. Swartzlander, Jr., "A Fused Floating-Point Four-Term Dot Product Unit," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 63, March 2016, pp. 370-378.

Fei Zhou, Lauren Guckert, Yao-Feng Chang, Earl E. Swartzlander, Jr., and Jack Lee, "Bidirectional Voltage Based Implication Operations Using SiO_x Based Unipolar Memristors," *Applied Physics Letters,* vol. 107, November 2015, paper 183501.

Weiqiang Liu, and Earl E. Swartzlander, Jr., "Design of 3-D Quantum-dot Cellular Automata Adders*," IEICE Electronics Express*, vol. 12, no. 6, pp. 1587-1591, 2015.

Inwook Kong, Seong-Wan Kim, and Earl E. Swartzlander, Jr., "Design of Goldschmidt Dividers With Quantum-Dot Cellular Automata," *IEEE Transactions on Computers*, vol. 63, October 2014, pp. 2620-2625.

Jongwook Sohn and Earl E. Swartzlander, Jr., "A Fused Floating-Point Three-Term Adder," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 61, October 2014, pp. 2842-2850.

Weiqiang Liu*,* Liang Lu, Máire O'Neill*,* and Earl E. Swartzlander, Jr., "A First Step Toward Cost Functions for Quantum-Dot Cellular Automata Designs," *IEEE Transactions on Nanotechnology*, vol. 13, May 2014, pp. 476-487.

Earl E. Swartzlander, Jr., "STARS: Electronic Calculators: Desktop to Pocket," *Proceedings of the IEEE*, vol. 101, December 2013, pp. 2558-2562.

Liang Lu, Weiqiang Liu, Máire O'Neill, and Earl E. Swartzlander Jr., "QCA Systolic Array Design," *IEEE Transactions on Computers*, vol. 62, March 2013, pp. 548-560.

Samuel I. Ward, Myung-Chul Kim, Natarajan Viswanathan, Zhuo Li, Charles J. Alpert, Earl E. Swartzlander, Jr., and David Z. Pan, "Structure-Aware Placement Techniques for Designs with Datapaths," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, February 2013, pp. 228-241.

Hyesook Lim, Changhoon Yim, and Earl E. Swartzlander, Jr., "Priority Area-based Quad-Tree Packet Classification Algorithm and Its Mathematical Framework," *Applied Mathematics & Information Sciences*, vol. 7, no. 1, 2013, pp. 9-20.

Weiqiang Liu, Saket Srivastava, Liang Lu, Maire O'Neill, and Earl E. Swartzlander Jr., "Are QCA Cryptographic Circuits Resistant to Power Analysis Attack?" *IEEE Transactions on Nanotechnology*, vol. 11, November 2012, pp. 1239-1251.

Jongwook Sohn and Earl E. Swartzlander, Jr., "Improved Architectures for a Fused Floating-Point Add-Subtract Unit," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 59, October 2012, pp. 2285-2291.

Hyesook Lim, Soohyun Lee, and Earl E. Swartzlander, Jr., "A new hierarchical packet classification algorithm," *Computer Networks*, vol. 56, no. 13, September 2012, pp. 3010-3022.

Earl E. Swartzlander, Jr. and Hani H. Saleh, "FFT Implementation with Fused Floating-Point Operations," *IEEE Transactions on Computers*, vol. 61, February 2012, pp. 284-288.

Waqas Akram and Earl E. Swartzlander, Jr.," Tunable Mismatch Shaping for Quadrature Bandpass Delta-Sigma Data Converters," *Journal of Signal Processing Systems for Signal, Image, and Video Technology*, vol. 65, no. 2, November 2011, pp. 199-210.

Weiqiang Liu, Liang Lu, Maire O'Neill, Earl E. Swartzlander Jr., and Roger Woods, "Design of Quantum-dot Cellular Automata Circuits Using Cut-Set Retiming," *IEEE Transactions on Nanotechnology*, vol. 10, September 2011, pp. 1150-1160.

Inwook Kong and Earl E. Swartzlander, Jr., "A Goldschmidt Division Method with Faster than Quadratic Convergence," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, April 2011, pp. 696-700.

Inwook Kong and Earl E. Swartzlander, Jr., "A Rounding Method to Reduce the Required Multiplier Precision for Goldschmidt Division," *IEEE Transactions on Computers*, *IEEE Transactions on Computers*, vol. 59, December 2010, pp. 1703-1708.

Ron S. Waters and Earl E. Swartzlander, Jr., "A Reduced Complexity Wallace Multiplier Reduction," *IEEE Transactions on Computers*, *IEEE Transactions on Computers*, vol. 59, August 2010, pp. 1134-1137.

Hyesook Lim, Changhoon Yim and Earl E. Swartzlander, Jr., "Priority Tries for IP Address Lookup," *IEEE Transactions on Computers*, vol. 59, June 2010, pp. 784-794.

Terence Rodrigues and Earl E. Swartzlander, Jr., "Adaptive CORDIC: Using Parallel Angle Recoding to Accelerate Rotations" *IEEE Transactions on Computers*, vol. 59, April 2010, pp. 522-531.

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Earl E. Swartzlander, Jr., "Merged Arithmetic for Signal Processing," *Proceedings of the 4th Symposium on Computer Arithmetic*, Santa Monica, CA, 1978, pp. 239-244.

Earl E. Swartzlander, Jr., "Microprogrammed Control for Signal Processing," *Proceedings of the 10th Workshop on Microprogramming*, Niagara Falls, NY, 1977, pp. 80-84.

E. E. Swartzlander, Jr. and B. K. Gilbert, "High-Speed Computerized Tomography," *Proceedings of the SPIE International Optical Computing Conference*, Vol. 119, 1977, pp. 299-306.

J. L. Buie and E. E. Swartzlander, Jr., "High Density Bipolar Logic Technology," *COMPCON Proceedings*, San Francisco, CA, Spring 1977, pp. 338-341.

B. K. Gilbert, R. D. Beistad, E. E. Swartzlander, Jr., L. M. Kruger, A. Chu, D. R. Breuer and E. L Ritman, "Development of Very High-Speed Multi-Axial Tomographic Algorithms

Employing Digital High Capacity Fixed Point Arithmetic Hardware," *Proceedings of the San Diego Biomedical Symposium*, New York: Academic Press, 1977, pp. 159-168.

R. P. Cheung, K. Wayne Current and Earl E. Swartzlander, Jr., "A Very High Speed Digital Correlation Technique," *Proceedings of the National Telecommunications Conference*, 1976, pp. 52.4-1-52.4-5.

Earl E. Swartzlander, Jr., "Applications of the Inner Product Computer," *Proceedings of the ACM Annual Conference*, Atlanta, GA, 1973, pp. 97-100.

Earl E. Swartzlander, Jr., "Models for Thermistor Characteristics," *Proceedings of Cal-Poly Measurement Science Conference*, San Luis Obispo, CA, December 1972.

Earl E. Swartzlander, Jr., "Comparison of Temperature Sensors for Space Instrumentation," in H. H. Plumb, ed., *Temperature - Its Measurement and Control in Science and Industry*, Vol. 4, pt. 3, Pittsburgh: Instrument Society of America, 1971, pp. 2337-2345.

Earl E. Swartzlander, Jr., "Comparison of Temperature Sensors for Space," *Proceedings of Cal-Poly Measurement Science Conference*, San Luis Obispo, CA, November 1970, pp. 122-131.

Earl E. Swartzlander, Jr., "Comparison of Temperature Sensors for Apollo Experiment Instrumentation," *ISA Advances in Instrumentation*, Vol. 24, Houston, TX, October 27-30, 1969, Paper 665.

Earl E. Swartzlander, Jr., "Absolute and Differential Temperature Monitors for Apollo Space Experiments," International Geoscience Electronics Symposium, Washington, DC, April 1969.

Seminars (36):

"Fused Floating-Point Arithmetic for DSP Applications," IEEE San Fernando Valley Section, California State University at Northridge, March 17, 2010.

"The Seven Wonders of Computer Arithmetic," (Distinguished Lecture), Iowa State University, October 15, 2009.

"Digital Multiplier Performance," IEEE Solid-State Circuits Society, Austin Section, September 9, 2008

"Fast Multiplier Design," Queen's University of Belfast, Institute of Electronics, Communications and Information Technology, Distinguished Scholar Lecture, June 21, 2007.

"Adder Design in Quantum-dot Cellular Automata," Queen's University of Belfast, Institute of Electronics, Communications and Information Technology, Distinguished Scholar Lecture, June 19, 2007.

"The Case for Application Specific Computers," Southern Methodist University, Department of Computer Science and Engineering, Distinguished Lecture, November 15, 2001.

"The Seven Wonders of Computer Arithmetic," (Birck Distinguished Seminar) Purdue University, December 15, 1998.

"Computer Arithmetic," (Guest Lecture) Southern Methodist University, March 21, 1996.

"Wafer Scale Integration," University of Texas at Dallas, March 21, 1996.

"Advanced Technologies for Systems on Silicon," University of California at Santa Barbara, April 21, 1995

"Industry-Academic Collaboration in Computer Engineering," Symposium on the 40th anniversary of the creation of the first center for scientific calculating in Italy, Politecnico di Milano, Milan, Italy, February 20, 1995.

"Wafer Scale Integration," University of California, Davis, November 4, 1994, New York Academy of Science, May 17, 1994, Fallcon, Cedar Rapids, IA, November 4, 1993, University of Massachusetts, Amhurst, October 4, 1993, University of Louisville, April 22, 1993, and Hitachi Central Research Laboratory, Tokyo, Japan, March 29, 1993

"Efficient Arithmetic for Signal Processing," Austin Section of the IEEE Computer Society, November 16, 1992 and Texas A&M University Distinguished Lecture, October 6, 1992

"The Use of VLSI for Application Specific Computing," University of Southwestern Louisiana, April 9, 1992

"Wafer Scale Integration," North Carolina State University, March 16, 1992

"Wafer Scale Integration for Digital Signal Processing," Politecnico di Milano, Milan, Italy, July 10, 1991

"Wafer Scale Integration," Queens University of Belfast, Northern Ireland, July 2, 1991

"Wafer Scale Integration for Digital Signal Processing," University of Southwestern Louisiana Distinguished Lecture, March 22, 1991

"Wafer Scale Integration," University of California at San Diego, Spring, 1990, University of Arizona, Spring, 1990, Duke University, Spring, 1990, University of Texas at Austin, Spring, 1990, and University of Southern California, September, 1987

"High Speed FFT Processor Implementation," McMaster University, Toronto, Ontario, Canada, June 7, 1985

"VLSI: The Technology of Supercomputers," George Mason University, October 12, 1983

"VLSI Signal Processor Implementation," Aerospace Corp., September 16, 1983

"VLSI Architecture," University of Minnesota, March 10, 1981, University of Illinois, April 16, 1980, and University of Southern California, November 28, 1979

"Microprocessors," TRW Colloquium, March 28, 1978

Short Course and Tutorial Presentations (49):

"Advanced Computing and Sensors," Senior Service Lecture, University of Texas at Austin Continuing Engineering Studies, February 24, 2004, October, 2002, October 17, 2001, October 3, 2000, October 14, 1999, October 15, 1998, November 18, 1997, and October 17, 1996

"Fundamentals of Computer Design, Performance and Cost," Engineering and Technology Institute, University of Texas at Austin Continuing Engineering Studies, September 12, 1996

"Computer Performance and Cost," and "ALU Design," IBM Austin Technical Refresher Course, University of Texas at Austin Continuing Engineering Studies, January 19, 1996

"Advanced Computing and Sensors," Senior Service Lecture, University of Texas at Austin Continuing Engineering Studies, October 17, 1995

"Computer Performance and Cost," and "ALU Design," IBM Austin Technical Refresher Course, University of Texas at Austin Continuing Engineering Studies, October 13, 1995

"Fundamentals of Computer Design, Performance and Cost," Engineering and Technology Institute, University of Texas at Austin Continuing Engineering Studies, May 11, 1995

"Sensor Signal Processing," Senior Service Lectures, University of Texas at Austin Continuing Engineering Studies, November 29, 1994 and December 1, 1994

"Logic Design and Arithmetic Circuits," Engineering and Technology Institute, University of Texas at Austin Continuing Engineering Studies, August 11-12, 1994

"Advanced Signal Processing and Computing," Senior Service Lectures, University of Texas at Austin Continuing Engineering Studies, March 9 & 23, 1994

"Logic Design and Arithmetic Circuits," Engineering and Technology Institute, University of Texas at Austin Continuing Engineering Studies, September 9-10, 1993

"Advanced Signal Processing and Computing," Senior Service Lectures, University of Texas at Austin Continuing Engineering Studies, September 8 & 10, 1992

"Systolic Systems and Technology," Arc Educators, Killarney, Ireland, May 29-30, 1989 and San Diego, CA, May 23-24, 1988

"Semi-Custom Design of VLSI Circuits," IEEE Computer Society, Boston, MA, September, 1986 and IEEE Computer Society, Washington, DC, November 19, 1985

"The VLSI Design Challenge," Arc Educators, Los Angeles CA, August 14-17, 1984

"Advanced VLSI Design for Signal Processing Applications," DPMA Educational Foundation, Los Angeles CA, June 19, 1984

"Fundamentals of Digital Processing," and "Introduction to Digital Technologies," CIA-ORD Visiting Scholars Course, Washington, DC, March 6-7, 1984

"Signal Processing Architecture and Device Technology," Technology Transfer Society, Los Angeles CA, November 10, 1983, San Francisco, CA November 14, 1983

"VLSI Architecture and Applications," Technology Transfer Society, Newport Beach, CA, January 24-25, 1983, San Francisco, CA January 27-28, 1983, Phoenix, AZ, February 10-11, 1983, Paris, France, April 7-8, 1983, Copenhagen, Denmark, April 11-12, 1983, and London, UK, April 14-15, 1983

"Design of Embedded Computer Systems," Aerospace and Defense Conference, Los Angeles, CA, March 29, 1982 and Washington, DC May 24, 1982

"System Architecture," DPMA Short Course, London, UK, October 19-20, 1981

"Advanced Microprocessors: the Intel iAPX-432," University of Michigan, July 31, 1981

"VLSI Architectures," Palisades Institute, San Francisco, CA January 14, 1981

"VLSI Architecture," International Computer Symposium, Taipei, Taiwan, December 1980

"VLSI Architectures," Palisades Institute, Boston, MA, October 22, 1980

"Zilog Z-8000 Microprocessor," University of Michigan, August 1, 1980

"VLSI Architecture," American University, Washington, DC, June 3, 1980

"Bipolar VLSI for Signal Processing," University of Maryland, April 7, 1980 and UCLA, May 22, 1980 and September 18, 1980

"Design of Custom Microelectronic Devices," MINI/MICRO-79, Anaheim, CA, September 26, 1979 and Los Angeles, CA, November 28, 1979

"Zilog Z-8000 Microprocessor," University of Michigan, August 3, 1979

"VLSI Architecture," American University, Washington, DC, June 4, 1979

Short Courses Organized and Coordinated:

TI Temple, TX Technical Refresher Course, October, 1996-February, 1997, (13 days, 13 lecturers)

Engineering and Technology Institute, University of Texas at Austin Continuing Engineering Studies, September 12-14, 1996, (2.5 days, 4 lecturers)

IBM Austin Technical Refresher Course, University of Texas at Austin Continuing Engineering Studies, January-April, 1996, (10 days, 11 lecturers)

IBM Austin Technical Refresher Course, University of Texas at Austin Continuing Engineering Studies, October, 1995-February, 1996, (10 days, 11 lecturers)

Engineering and Technology Institute, University of Texas at Austin Continuing Engineering Studies, May-August, 1995, (10 days, 10 lecturers)

Introduction to Systolic and Array Processing, Arc Educators, Killarney, Ireland, May 29-30, 1989, (2 days, 4 lecturers)

Introduction to Systolic and Array Processing, Arc Educators, San Diego, CA, May 23-24, 1988, (2 days, 4 lecturers)

VLSI Design Technology, Arc Educators, Los Angeles CA, August 14-17, 1984, (4 days, 8 lecturers)

Ph.D. Students Supervised (46):

Waqas Akram, "Tunable Mismatch Shaping For Bandpass Delta-Sigma Data Converters," May 2011

Jason Todd Arbaugh, "Table Look-Up CORDIC: Effective Rotations Through Angle Partitioning," December 2004

Edwin de Angel, "Low Power Digital Multiplication," December 1996

Robert John Ascott, "JAVAFLOW: A Java Dataflow Machine," December 2014

K'Andrea C. Bickerstaff, "Optimization of Column Compression Multipliers," August 2007

Tom Callaway, "Area, Delay, and Power Modeling of CMOS Adders and Multipliers," December 1996

Heumpil Cho, "Adder and Multiplier Design and Analysis in Quantum-dot Cellular Automata," December 2006

Gwangwoo Choe, "Merged Arithmetic for Wavelet Transforms," December 2000

Youngmoon Choi, "Parallel Prefix Adder Design," December 2004

Jae hun Choi, "High Speed and Low Area Techniques for Computer Arithmetic Operations," December 2000

Ayman El-Khashab, "Modular Pipeline Fast Fourier Transform Algorithm," May 2003

Kurt Alan Feiste, "Merged Arithmetic for Digital Signal Processing," December 1999

Jay Fletcher, "Control and Implementation of Integrated Voltage Regulators," December 2013

William Lynn Gallagher, "Fault Tolerant Multipliers and Dividers Using Time Shared Triple Modular Redundancy," December 1999

Luaren Elise Guckert, "Memristor-Based Arithmetic Units," December 2016

Yuang-Ming Hsu, "Concurrent Error Correcting Arithmetic Processors," August 1995

Jae Hoon Jeong (co-supervised with Tony Ambler), "Efficient Verification/Testing of System-on-Chip through Fault Grading and Analog Behavioral Modeling," December 2013

Kihwan Jun, "Improved Algorithms for Non-restoring Division and Square Root," December 2012

Chang Yong Kang, "CORDIC-Based High-Speed Direct Digital Frequency Synthesis," May 2003

Mohammad S. Khan, "Design of an Interface Control Unit for Rapid Prototyping," August 1995

Seong-Wan Kim, "Design of Parallel Multipliers and Dividers in Quantum-Dot Cellular Automata," May 2011.

Inwook Kong, "Improved Algorithms and Hardware Designs for Division by Convergence," December 2009

Jae-Hyuck Kwak, "High Speed CORDIC Processor Designs: Algorithms, Architectures, and Applications," May 2000

Wai Ming Hercule Kwan (co-supervised with Ed Powers), "Parallel Implementation of a Fast Third-Order Volterra Digital Filter," August 1998

Ohsang Kwon, "On High-Performance Multiplier Design Using Dynamic CMOS Circuits," December 2000

Hyesook Lim, "Multi-Dimensional Systolic Arrays and Their Implementations for Discrete Fourier Transform and Discrete Cosine Transform," December 1996

Jae Hong Min, "Fused Floating-Point Arithmetic for Application Specific Processors," December 2013

Bassam Jamil Mohd, "Switch-Based Fast Fourier Transform Processor" December 2008

Hyuk Park, "Truncated Multiplications and Divisions for the Negative Two's Complement Number System," December 2007

Tung Nang Pham, "Design of Radix-4 Dividers Using High Redundancy in 65 Nanometer CMOS Technology," December 2005

Eric C. Quinnell, "Floating-Point Fused Multiply-Add Architectures," May 2007

Giri N. K. Rangan, "A Fractional-N Frequency Synthesizer for an Adaptive Network Backplane Serial Communication System," December 2005

Nagaraja Revanna, "Memristor Based Arithmetic Circuit Design," December 2016

Moises Emanuel Robinson, "Low-Noise and High-Frequency Clock Generation Core for VLSI CMOS Integration," December 2005

Terence Keith Rodrigues, "Adaptive CORDIC: Using Parallel Angle Recoding to Accelerate CORDIC Rotations," December 2007

Hani Hasan Mustafa Saleh, "Fused Floating-Point Arithmetic For DSP," May 2009

Moboluwaji O. Sanu, "Parallel Multipliers for Modular Arithmetic," December 2005

Michael J. Schulte, "A Variable Precision Interval Arithmetic Processor," May 1996

Jongwook Sohn, "Improved Architectures for Fused Floating-Point Arithmetic Units," May 2013

Michael B. Sullivan (co-supervised with Mattan Erez), "Low-Cost Duplication for Seperable Error Detection in Computer Arithmetic," May 2015

Shaohua Wan (co-supervised with Jake Aggarwal), "Learning to Recognize Egocentric Activities Using RGB-D Data," August 2015

Shaoyun Wang, "A CORDIC Arithmetic Processor," May 1998

Ronald S. Waters, "Total Delay Optimization for Column Reduction Multipliers Considering Non-Uniform Arrival Times to the Final Adder," May 2014

Jae Ki Yoo, "A Background Calibration Technique and Self Testing Method for the Pipeline Analog to Digital Converter," December 2004

Sungwook Yu, "VLSI Implementation of Multidimensional Discrete Fourier Transform and Discrete Cosine Transform," May 2000

Thomas A. Ziaja, "Characterization and Analysis of Type 1 Error in Circuit Test," May 1996

Masters Students Supervised (40):

Waqas Akram, "Direct Digital Frequency Synthesis Using Piece-wise Polynomial Approximation," May 2003

Ambica Ashok, "Comparison Study of Magnitude Comparators," December 2008

Ryan David Bullard, "Parallel-Prefix Addition," August 2004

Thomas K. Callaway, "High-Speed SRT Division," August 1992

Wesley Donald Chu, "Wallace and Dadda Multipliers Implemented Using Carry Lookahead Adders," December 2013

Sumant Dalmiya, "A Comparative Study of Adders," December 2015

Albert Neil Danysh, "Interference-Based Hardware Architectures to Compute Real-Time Holograms," May 1999

Poulami Das, "A Comparative Study of Adders," May 2016

Marlin W. Frederick, Jr., “CORDIC Algorithms Using Internal Signed-Digit Representations,” December 1993

Nakshatra Gajbhiye, “Design of Final Adder Stage of Dadda Multiplier,” May 2008

Ratika Goyal, “A 53 by 53 bit Significand Multiplier Implementation for a Double-precision Floating-point Multiplier,” August 2008

Robert T. Grisamore, “Sign Extension for Parallel Adders and Multipliers Using Negative Save,” December 2003

Scott T. Haban, “A VLSI Module to Compute the Inverse Discrete Cosine Transform for MPEG-2 Video Decompression,” December 1994

Dylan A. Hester, “Noise Management of Isochronous Digital Activity in an Audio Digital to Analog Converter,” May 1999

Reid Hewlitt, “High-Speed Source-Synchronous LVDS Pin Electronics and New Architectures for Automatic Test Equipment,” December, 2001

Robert F. Jones, Jr., “Formal Verification Techniques and Industry Application,” December 1993

Kihwan Jun, “Modified Non-restoring Division Algorithm with Improved Delay Profile,” May 2011

Panjin Kim, “High Speed Multipliers Implemented with Carry Lookahead Adders,” May, 2010

Eric J. King, “A Reduced Complexity Truncated Multiplier,” August 1998

Kafai Leung, “Digital Filters for a 120 dB Delta-Sigma Analog-to-Digital Converter System,” May 1997

Tom Lynch, “Binary Adders,” May 1996

James McIntosh, “High-Speed Cosine Generator,” May 1996

Jae Hong Min, “Low-Power Fused FFT Butterfly Arithmetic Unit With Merged Multiple-Constant Multiplier,” December 2010

Vignesh Naganathan, “A Comparative Analysis of Parallel Prefix Adders in 32nm and 45nm Static CMOS Technology,” May 2015

Nidhi Nayyar, “Graphic Specific Processing – An Overview,” May 2008

Hyuk Park, “Partially Merged Arithmetic Implemented with Two-Term Modules,” May 2002

Kara Basden Pepe, “A Comparative Analysis of an Asynchronous and a Synchronous Multiplier-Accumulator Design,” August 1994

Tung Pham, “A True LRU Design for a Four-Way Set Associative Cache in a High-Performance Low-Power System on Chip,” August 2000

Anusha Ravi, “Delay Analysis of Dadda and Wallace Reduction Techniques,” December 2007

Devika Ray, “Implementation and Comparison of High Speed Dividers,” August 2008

Robert B. Richert, “A 32 Bit RISC Core for a Gigabit-Plus Network Processor,” August 1999

Michael J. Schulte, “Algorithms and Hardware Designs for Parallel Elementary Function Generation,” December 1992

Ankith Shanthiraj, "Design of Circuits for Sub-Threshold Voltages: Implementation of Adders," May 2016

Jongwook Sohn, "Improved Architectures for a Fused Floating-Point Add-Subtract Unit," December 2011

Srivatsan Sridharan, "Design of Fast Multipliers Using Modified Adder Circuits," August 2007

Jonathan Barten Stanley, "Tradeoffs in Parallel Prefix Adder Structures," May 2015

Jian Tao, "Survey On Fast Floating Point Addition," December 2005

Samuel Isaac Ward, "Timing Optimization through Statistical Latch Cloning Selection," December 2007

Thomas A. Ziaja, "A Review of VLSI and Board Test Design," May 1992

Roberto Francisco Zuniga, "Adder Designs in VLSI," December 2001,

Current Ph.D. Students:

Admitted to Candidacy

Shaohua Wan Wan (co-supervised with Jake Aggarwal), Learning to Recognize Egocentric Actions using RGBD Data

Not yet Admitted to Candidacy

Dustyn Blasig
Charles Corley
Trenton Grale
Mike O'Connor
Karthik Sundaram

Courses Taught:

Spring, 2014	EE 411 Circuit Theory, I EE 225 Co-Op Internship Supervision EE 464 Senior Design Project
Fall, 2014	EE 411 Circuit Theory, I EE 382N High-Speed Computer Arithmetic-1 EE 225 Co-Op Internship Supervision
Summer, 2014	EE 225 Co-Op Internship Supervision
Spring, 2014	EE 411 Circuit Theory, I EE 225 Co-Op Internship Supervision EE 464 Senior Design Project
Fall, 2013	EE 382N High-Speed Computer Arithmetic-1 EE 225 Co-Op Internship Supervision EE 364D Senior Design Project
Summer, 2013	EE 225 Co-Op Internship Supervision

Spring, 2013	EE 411 Circuit Theory, I EE 225 Co-Op Internship Supervision
Fall, 2012	EE 382N High-Speed Computer Arithmetic-1 EE 225 Co-Op Internship Supervision
Summer, 2012	EE 225 Co-Op Internship Supervision
Spring, 2012	EE 411 Circuit Theory, I EE 225 Co-Op Internship Supervision
Fall, 2011	EE 382N High-Speed Computer Arithmetic-1 EE 225 Co-Op Internship Supervision
Summer, 2011	EE 225 Co-Op Internship Supervision
Spring, 2011	EE 411 Circuit Theory, I EE 382M Application Specific Processor Design EE 225 Co-Op Internship Supervision
Fall, 2010	EE 382N High-Speed Computer Arithmetic-1
Spring, 2010	EE 411 Circuit Theory, I
Fall, 2009	EE 382N High-Speed Computer Arithmetic-1
Spring, 2009	EE 411 Circuit Theory, I EE 382M Application Specific Processor Design
Fall, 2008	EE 382N High-Speed Computer Arithmetic-1
Spring, 2008	EE 411 Circuit Theory, I EE 382M Application Specific Processor Design
Fall, 2007	EE 382N High-Speed Computer Arithmetic-1
Spring, 2007	EE 411 Circuit Theory, I EE 382V Floating-Point Arithmetic
Fall, 2006	EE 382N High-Speed Computer Arithmetic-1
Spring, 2006	EE 411 Circuit Theory, I EE 397K Floating-Point Arithmetic
Fall, 2005	EE 382N High-Speed Computer Arithmetic-1
Spring, 2005	EE 411 Circuit Theory, I
Fall, 2004	EE 382N High-Speed Computer Arithmetic-1 EE 382N High-Speed Computer Arithmetic-2
Spring, 2004	EE 411 Circuit Theory, I
Fall, 2003	EE 382N High-Speed Computer Arithmetic-1 EE 382N High-Speed Computer Arithmetic-2
Spring, 2003	EE 411 Circuit Theory, I
Fall, 2002	EE 382N High-Speed Computer Arithmetic
Spring, 2002	EE 382N High-Speed Computer Arithmetic

Fall, 2001	EE 306 Introduction to Computer Engineering
Spring, 2001	EE 362M Application Specific Processing
Fall, 2000	EE 382N High-Speed Computer Arithmetic
Spring, 2000	EE 362M Application Specific Processing
Fall, 1999	EE 382N High-Speed Computer Arithmetic EE 382N Advanced Topics in Computer Arithmetic
Spring, 1999	EE 362M Application Specific Processing
Fall, 1998	EE 382N High-Speed Computer Arithmetic EE 397K Seminar on Advanced Computer Arithmetic
Spring, 1998	EE 362N Computer Architecture
Fall, 1997	EE 382N High-Speed Computer Arithmetic
Spring, 1997	EE 362N Computer Architecture
Fall, 1996	EE 382N High-Speed Computer Arithmetic EE 397K Seminar on Advanced Computer Arithmetic
Spring, 1996	EE 362N Computer Architecture
Fall, 1995	EE 382N High-Speed Computer Arithmetic EE 397K Seminar on Advanced Computer Arithmetic
Spring, 1995	EE 362N Computer Architecture
Fall, 1994	EE 382N High-Speed Computer Arithmetic EE 397K Seminar on Advanced Computer Arithmetic
Spring, 1994	EE 382N High-Speed Computer Arithmetic EE 362N Computer Architecture
Fall, 1993	EE 382N High-Speed Computer Arithmetic
Spring, 1993	EE 382N High-Speed Computer Arithmetic EE 397K Seminar on Advanced Computer Arithmetic
Fall, 1992	EE 382N High-Speed Computer Arithmetic EE 411 Network Theory, I
Spring, 1992	EE 382N High-Speed Computer Arithmetic EE 397K Seminar on Advanced Computer Arithmetic
Fall, 1991	EE 382N High-Speed Computer Arithmetic
Spring, 1991	EE 382N High-Speed Computer Arithmetic
Fall, 1990	EE 382N High-Speed Computer Arithmetic

CONTRACTS:

At the University of Texas at Austin:

Unrestricted Grant, AMD, Inc., 2012-2013, $50K, Principal Investigator.

Unrestricted Grant, AMD, Inc., 2011-2012, $50K, Principal Investigator.

Unrestricted Grant, AMD, Inc., 2010-2011, $50K, Principal Investigator.

Unrestricted Grant, AMD, Inc., 2006-2007, $15K, Principal Investigator.

Fellowship (Jaeki Yoo/Giri Rangan) Silicon Laboratories, Inc., 2004-2005, $22K.

Fellowship (Jaeki Yoo) Silicon Laboratories, Inc., 2003-2004, $32K.

Fellowship (Jaeki Yoo) Silicon Laboratories, Inc., 2002-2003, $30K.

Fellowship (Jaeki Yoo) Silicon Laboratories, Inc., 2001-2002, $30K.

High Performance Digital Signal Processors, Texas Higher Education Coordinating Board, Advanced Technology Program, ATP-403, 2000-2001, $103K, Co-Principal Investigator.

Fellowships (K'Andrea Bickerstaff and Gwangwoo Choe/Chang Yoon Kang) Cirrus Logic, Inc., 2000-2001, $46K.

Fellowship (Jaeki Yoo) Silicon Laboratories, Inc., 2000-2001 $30K.

Fellowship (Robert Richert) Silicon Laboratories, Inc., 2000, $15K.

Fellowships (K'Andrea Bickerstaff and Lynn Gallagher/Gwangwoo Choe) Cirrus Logic, Inc., 1999-2000, $46K.

High Performance Digital Signal Processors, Texas Higher Education Coordinating Board, Advanced Technology Program, ATP-403, 1998-1999, $135K, Co-Principal Investigator.

Fellowships (K'Andrea Bickerstaff and Lynn Gallagher) Crystal Semiconductor Corp., 1998-1999, $46K.

Unrestricted Grant, Rockwell Foundation, 1995-1997, $40K, Principal Investigator.

Fellowship (Shaoyun Wang), Crystal Semiconductor Corp., 1995-1997, $64K.

Fellowship (K'Andrea Bickerstaff), Crystal Semiconductor Corp., 1995-1997, $64K.

Fellowship (Meng-Jang Lin), Motorola, 1995, $20K.

Fellowship (Edwin De Angel), Crystal Semiconductor Corp., 1994-1996, $40K.

High-Performance, Low-Power Signal Processors, Office of Naval Research, Grant No. N00014-92-K-2000, 1992-1994, $52K, Co-Investigator with Professor H. G. Cragon.

Faculty Assistantship (Suzanne Barber), TRW Foundation, 1992-1995, $45K.

Fellowship (Mike Schulte), TRW Foundation, 1992-1995, $21K.

Faculty Assistantship (Vijay Garg and Joydeep Ghosh), TRW Foundation, 1991-1994, $45K.

Fellowship (Tom Callaway), TRW Foundation, 1991-1994, $20K.

"IEEE Transactions on Computers Editorial Support," IEEE Computer Society, 1991-1995, $220K.

At TRW:

Modular Transform Processor, Maryland Procurement Office, 1983-1984, $300K, Principal Investigator

FFT Processor, TRW IR&D, 1982-1983, $200K, Principal Investigator

Distributed Processing Design Technology Development, Ballistic Missile Advanced Technology Office, 1980-1982, $1,000K, Principal Investigator

Sonar Adaptive Equalizer, TRW Washington Operations, 1978, $70K, Principal Investigator

High-Speed Micro Signal Processor, Air Force Avionics Laboratory, Contract F33615-76-C-1249, June 1976-December 1976, $82K, Principal Investigator