CURRICULUM VITAE - Yale N. Patt

PERSONAL

Yale N. Patt
901 W. 9th Street, Suite 603, Austin, TX 78703
(or, The University of Texas at Austin, Electrical & Computer Engineering Department,
2501 Speedway, EER 5.802
Austin, TX 78712

EDUCATION

Northeastern University, B.S. in Electrical Engineering, June 1962

Stanford University, M.S. in Electrical Engineering, June 1963

Stanford University, Ph.D. in Electrical Engineering, June 1966

PRIMARY EMPLOYMENT (Since obtaining the PhD)

Professor of Electrical and Computer Engineering, and	
Ernest Cockrell, Jr. Centennial Chair in Eng'g at UT Austin	7/99-present
University Distinguished Teaching Professor, UT Austin	10/11-present
Professor of Electrical Eng'g & Computer Science, University of Michigan	11/88-6/99
Visiting Professor, Elec. Eng'g & Computer Science, U.C. Berkeley	9/79-8/88
Professor of Computer Science and Mathematics, S.F. State University	8/76-6/89
Associate Professor of Computer Science and E.E., N.C. State University	1/69-5/76
Captain, U.S. Army, serving on active duty	6/67-6/69
Assistant Professor of Electrical Engineering, Cornell University	9/66-6/67

HONORS AND AWARDS

Member, National Academy of Engineering, elected: 2014.

1996 IEEE/ACM Eckert-Mauchly Award "for important contributions to instruction level parallelism and superscalar processor design." (The IEEE/ACM Eckert-Mauchly Award is the highest honor in the field of computer architecture.

Benjamin Franklin Medal in Computer and Cognitive Science, presented by the Franklin Institute, April, 2016.

2000 ACM Karl V. Karlstrom Outstanding Educator Award, "for great ability, dedication, and success in developing computer science education, and for outstanding achievements as a teacher." (The Karlstrom Award is the highest award for computer educators presented by the ACM.)

1995 IEEE Emanuel R. Piore Award (the IEEE Technical Field Medal for Information Processing), "for contributions to computer architecture leading to commmercially viable high performance microprocessors."

2013 IEEE Harry H. Goode Award "for nearly half a century of significant contributions to information processing, including microarchitecture insights, a breakaway textbook, and mentoring future leaders."

1999 IEEE Wallace W. McDowell Award, "for your impact on the high performance microprocessor industry via a combination of important contributions to both engineering and education."

2011 IEEE B. Ramakrishna Rau Award (first recipient), "for significant contributions and inspiring leadership in the microarchitecture community with respect to teaching, mentoring, research, and service."

2005 IEEE Charles Babbage Award, "for fundamental contributions to high performance processor design."

2017 Friar Centennial Teaching Fellowship, presented by The University of Texas Friar Society, "in recognition of his excellence in and dedication to undergraduate teaching." (The Friars Centennial Teaching Award is the highest award for undergraduate teaching at the University of Texas.)

Honorary Doctorate, University of Belgrade, 2009, "for fundamental contributions to microprocessor design."

Honorary Professor, Zhejiang University, May, 2017.

Fellow, IEEE, for "Innovative contributions to the implementation of high performance computer architectures."

Fellow, ACM, for "many outstanding seminal contributions to high performance microarchitecture and for leadership and teaching in computer science and engineering education.

IEEE/ACM 2014 Inaugural Test of Time Influential Paper Award. The inaugural award identified ten papers from the first 25 years of the annual IEEE/ACM Microarchitecture Symposium (1968-1992) for the award. Four of the papers were: "HPS, a New Microarchitecture: Rationale and Introduction" (1985), with Wen-mei Hwu and Michael Shebanow, "Critical Issues Regarding HPS, a High Performance Microarchitecture" (1985), with Stephen Melvin, Wen-mei Hwu, and Michael Shebanow, "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines" (1988), with Stephen Melvin and Michael Shebanow, and "Two-level Adaptive Training Branch Prediction" (1991), with Tse-Yu Yeh.

ACM International Conference on Supercomputing 25th Anniversary volume of top papers published in that conference during its first 25 years included "Increasing the Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache" (1993), with Deborah Marr and Tse-Yu Yeh.

IEEE/ACM 2007 ISCA Most Influential Paper of the Year Award, for "the paper published in ISCA in 1992 that has had the most impact on the field (in terms of research, development, products or ideas) during the 15 years since it was published." For: "Alternative Implementations of Two-Level Adaptive Branch Prediction."

Elected to The University of Texas Academy of Distinguished Teachers, 2011 (see http://www.utexas.edu/faculty/academy/about/).

IEEE Third Millenium Medal, April, 2000.

IEEE Computer Society Golden Core Award, 1996.

ACM SigMICRO Distinguished Service Award, 2016.

Outstanding Lecturer of the Year, National ACM Lectureship Program, 2000-01.

Outstanding Lecturer of the Year, National ACM Lectureship Program, 1998-99.

Texas Excellence Teaching Award, presented by the Texas Exes (the Univerity's Alumni Association), selected by the Engineering Student Council, 2002.

Dad's Association Centennial Teaching Fellowship, The University of Texas at Austin, Fall semester, 2002.

Selected by the Student Engineering Council, UT Austin, as the Outstanding ECE Professor of the Year, 2007, 2009, 2014, 2016.

Appointed Arthur F. Thurnau Professor at the University of Michigan, March, 1998, "for his excellence in teaching and his dedication to undergraduate students."

Member, Sigma Xi, Tau Beta Pi, Eta Kappa Nu Honor Societies.

National Tau Beta Pi Fellow, 1962-1963.

1997 Research Excellence Award, University of Michigan, Dept of Electrical Engineering and Computer Science.

1996 Outstanding Teacher Award, University of Michigan, College of Engineering.

1995 Teaching Excellence Award, University of Michigan, Dept of Electrical Engineering and Computer Science.

Outstanding Professor of the Year, 1991-1992, selected by the Michigan student chapter of Eta Kappa Nu.

Best Paper Award, Micro-45, Vancouver, December, 2012, for "MorphCore: An Energy-Efficient Microarchitecture for High Performance ILP and High Throughput TLP," (with Khubaib, M. Aater Suleman, Milad Hashemi, and Chris Wilkerson).

Best Paper Award, ASPLOS XV, Pittsburgh, PA, March, 2010, for "Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems," (with Eiman Ebrahimi, Chang Joo Lee, and Onur Mutlu).

IEEE Micro Top Picks Special Issue Paper for papers published in 2010. Data Marshaling for Multi-core Architectures, *IEEE Micro*, Top Picks Special Issue, January/February, 2011. (with M. Aater Suleman, Onur Mutlu, Jose Joao, and Khubaib).

IEEE Micro Top Picks Special Issue Paper for papers published in 2009. Accelerating Critical Section Execution with Asymmetric Multi-Core Architectures, *IEEE Micro*, Top Picks Special Issue, January/February, 2010. (with

Aater Suleman, Onur Mutlu, and Moinuddin Qureshi).

IEEE Micro Top Picks Special Issue Paper for papers published in 2007. Adaptive Insertion Policies for High-Performance Caching. *IEEE Micro*, Top Picks Special Issue, January/February, 2008. (with Moinuddin K. Qureshi, Aamer Jaleel, Simon C. Steely Jr., and Joel Emer).

IEEE Micro Top Picks Special Issue Paper for papers published in 2006. Diverge-Merge Processor: Generalized and Energy-Efficient Dynamic Predication, *IEEE Micro*, Top Picks Special Issue, January/February, 2007, (with Hyesoon Kim, Jose Joao, and Onur Mutlu).

IEEE Micro Top Picks Special Issue Paper for papers published in 2005. Techniques for Efficient Processing in Runahead Execution Engines. *IEEE Micro*, Top Picks Special Issue, January/February, 2006, (with Onur Mutlu and Hyesoon Kim).

IEEE Micro Top Picks Special Issue Paper for papers published in 2005. Wish Branches: Combining Conditional Branching and Predication for Adaptive Predicated Execution, *IEEE Micro*, Top Picks Special Issue, January/February, 2006, (with Hyesoon Kim, Onur Mutlu, and Jared Stark).

IEEE Micro Top Picks Special Issue Paper for papers published in 2003. Runahead Execution: An Effective Alternative to Large Instruction Windows, *IEEE Micro*, Top Picks Special Issue, November/December, 2003. (with Onur Mutlu, Jared Stark, and Chris Wilkerson).

Best paper award in Hardware-Architecture at the 22nd Annual HICSS conference, January, 1989, "Tailoring Functional Units and Memory in a High Performance Prolog Architecture."

Best paper award in Hardware-Architecture at the 21st Annual HICSS conference, January, 1988, "HPSm2: A Refined Single Chip Microengine."

Best paper award in Hardware-Architecture at the 20th Annual HICSS conference, January, 1987, "A Clarification of the Dynamic/Static Interface."

Best paper award in Hardware-Architecture at the 19th Annual HICSS conference, January, 1986, "An HPS Implementation of VAX: Initial Design and Analysis."

PhD GRADUATES (MAJOR PROFESSOR)

Hamed El Lozy, PhD, North Carolina State University, 1973
Completeness Properties in m-Valued Logic

John Swensen, PhD, University of California, Berkeley, 1987
High-Bandwidth/Low-Latency Temporary Storage for Supercomputers

Wen-mei Hwu, PhD, University of California, Berkeley, 1987
HPSm: Exploiting Concurrency to Achieve High Performance in A Single-Chip Microarchitecture

Stephen Melvin, PhD, University of California, Berkeley, 1990
Performance Enhancement through Dynamic Scheduling and Large Execution Units in Single Instruction Stream Processors

Ashok Singhal, PhD, University of California, Berkeley, 1990
Exploiting Fine Grain Parallelism in Prolog

Chien Chen, PhD, University of California, Berkeley, 1991
Scheduling Heuristics and Runtime Data Structures for the Parallel Execution of PROLOG Programs

Michael Butler, PhD, University of Michigan, 1993
Aggressive Execution Engines for Surpassing Single Basic Block Execution

Tse-Yu Yeh, PhD, University of Michigan, 1993
Two-Level Adaptive Branch Prediction and Instruction Fetch Mechanisms for High Performance Superscalar Processors

Michael Shebanow, PhD, University of California, Berkeley, 1994
The Importance of Bus Transaction and Cache Consistency Protocol in the Design of High Performance Shared-Memory, Single-Bus Multiprocessor Systems

Robert Hou, PhD, University of Michigan, 1994
Improving Reliability and Performance of Redundant Disk Arrays by Improving Rebuild Time and Response Time

Gregory Ganger, PhD, University of Michigan, 1995
System-Oriented Evaluation of I/O Subsystem Performance

Bruce Worthington, PhD, University of Michigan, 1995
Aggressive Centralized and Distributed Scheduling of Disk Requests

Po-Yung Chang, PhD, University of Michigan, 1997
Classification-Directed Branch Predictor Design

Eric Hao, PhD, University of Michigan, 1998
Block Enlargement Optimizations for Increasing the Instruction Fetch Rate in Block-Structured Instruction Set Architectures

Sanjay Patel, PhD, University of Michigan, 1999
Trace Cache Design for Wide-Issue Superscalar Processors

Jared Stark IV, PhD, University of Michigan, 1999
Out-of-Order Fetch, Decode, and Issue

Marius Evers, PhD, University of Michigan, 1999
Improving Branch Prediction by Understanding Branch Behavior

Paul Racunas, PhD, University of Michigan, 2002
Reducing Load Latency through Memory Instruction Characterization

Robert Chappell, PhD, University of Michigan, 2003
Simultaneous Subordinate Microthreading

Mary Brown, PhD, The University of Texas at Austin, 2005
Reducing Critical Path Execution Time by Breaking Critical Loops

Onur Mutlu, PhD, The University of Texas at Austin, 2006
Efficient Runahead Execution Processors

Hyesoon Kim, PhD, The University of Texas at Austin, 2007
Adaptive Predication via Compiler-Microarchitecture Cooperation

Moinuddin Qureshi, PhD, The University of Texas at Austin, 2007
Adaptive Caching for High-Performance Memory Systems

Francis Tseng, PhD, The University of Texas at Austin, 2007
Braids: Out-of-Order Performance with Almost In-Order Complexity

Muhammad Aater Suleman, PhD, The University of Texas at Austin, 2010
An Assymetric Multi-Core Architecture for Efficiently Accelerating Critical Paths in Multithreaded Programs

Chang Joo Lee, PhD, The University of Texas at Austin, 2010

DRAM-Aware Prefetching and Cache Management

Eiman Ebrahimi, PhD, The University of Texas at Austin, 2011
Fair and High Performance Shared Memory Resource Management

Veynu Narasiman, PhD, The University of Texas at Austin, 2014
An Enhanced GPU Architecture for Not-So-Regular Parallelism with Special Implications for Database Search

Khubaib, PhD, The University of Texas at Austin, 2014
Performance and Energy Efficiency via an Adaptive MorphCore Architecture

Rustam Miftakhutdinov, PhD, The University of Texas at Austin, 2014
Performance Prediction for Dynamic Voltage and Frequency Scaling

Jose Joao, PhD, The University of Texas at Austin, 2014
Bottleneck Identification and Acceleration in Multithreaded Applications

Milad Hashemi, PhD, The University of Texas at Austin, 2016
On-Chip Mechanisms to Reduce Effective Memory Access Latency

KEYNOTE ADDRESSES

Keynote address, Perspectives on the Future of Computing, HiPEAC Computer Systems Week, Gothenburg, Sweden, May, 2018. Title: "Moore's Law, vonNeumann, Paradigms, Accelerators, Software, and Economics -- and what they mean to a Computer System."

Keynote address, 29th annual Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Campinas, Brazil, October, 2017. Title: "Processor Paradigms, Moore's Law, and Economics."

Keynote address, Workshop on Computer Architecture Education (WCAE 2017), in conjunction with ISCA, Toronto, June, 2017. Title: Computer Architecture Education: Black boxes proved harmful!

Keynote address, IEEE HPCA, First Workshop on Pioneering Processor Paradigms, Austin, February, 2017. Title: Processor Paradigms: Evolution or Revolution.

Keynote address, ACM/IEEE International Conference on Parallel Architectures and Compilation Techniques PACT2016), Haifa, Israel, September, 2016. Title: Greater Performance and Better Efficiency: Predicated Execution has shown us the way.

Keynote address, Shanghai Tech Workshop on Emerging Devices, Circuits and Systems (SWEDCS), Shanghai, July, 2016. Title: Energy-Efficient Computing: One more reason to tear down those walls.

Keynote address, IEEE COMPSAC 2016, 40th IEEE International Conference on Computers, Software & Applications, Atlanta, Georgia, June, 2016. Title: If Moore's Law does in fact end, whose job is it to pick up the slack? ...and How?

Keynote address, ACM International Conference on Supercomputing, Istanbul, June, 2016. Title: Performance = Bandwidth divided by Latency.

Keynote address, IEEE SMARTCOMP 2014, first international conference on Smart Computing, Hong Kong, November, 2014. Title: From DUMB Computers to SMART Computing.

Keynote address, 25st annual Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Porta de Galinhas, Brazil, October, 2013. Title: Parallelism: A serious goal or a silly mantra?

Keynote address, 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Istanbul, October, 2013. Title: The Run-time System: part of the O/S or part of the chip design?

Keynote address, International Conference on Supercomputing (ICS), Venice, June, 2012. Title: High Performance Supercomputers: should the individual processor be more than a brick?

Keynote address, IEEE System on a Chip Conference (SOCC 2011), Taipei, September, 2011. Title: Future Microprocessors: Return of the ASIC.

Keynote address, EE Times Virtual Event, "Multicore: Making Multicore Work for You," March, 2011. Title: Multi-core, Meganonsense and the Future, if we get it right.

Keynote address, First annual International Conference on Parallel, Distributed and Grid Computing (PDGC-2010), Waknaghat, Solan (HP), India, October, 2010. Title: The Microprocessor of 2020: Why you should care, and what you can do about it.

Keynote address, 21st annual Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Sao Paulo, Brazil, October, 2009. Title: The 1000 core microprocessor: Will we be ready for it?

Keynote address, College of Computing Research Day, Georgia Tech, September, 2009. Title: Future Microprocessors: Multi-core, Multi-nonsense, and What we must do differently moving forward.

Keynote address, Workshop on Integrating Parallellism Throughout the Undergraduate Computing Curriculum, in conjunction with PACT, Raleigh, NC, September, 2009. Title: Integrating Parallelism -- the tip of the iceberg.

Keynote address, International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS IX), July 2009, Samos. Title: Can we fix it? (part 2).

Keynote address, 7th annual ACS/IEEE International Conference on Computer Systems and Applications (AICCSA-2009), May, 2009, Rabat, Morocco. Title: Future Computer Systems and Applications: Revisiting Conventional Wisdom in the context of Multi-core and Many-core.

Keynote address, 22nd International Conference on Computing Systems (ARCS 2009), March, 2009, Delft. Title: The Challenges of Multicore: Information and Misinformation.

Keynote address, 15th IEEE International High Performance Computer Architecture Symposium (HPCA-15), February, 2009, Raleigh, N.C. Title: Multi-core demands Multi-interfaces.

Keynote address, European Union HiPEAC Summer School for PhD students in Computer Architecture and Embedded Systems (ACACES), July 2008, L'Aquila, Italy. Title: The Multi-core Era: What does it mean? (and even more importantly, what does it NOT mean?).

Keynote address, International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS VIII), July 2008, Samos. Title: Can it be fixed? Some thoughts after 40 years in the business.

Keynote address, 2008 IEEE International Conference on Networking, Architecture and Storage, June 2008, Chongqing, China. Title: The Microprocessor in the Year 2018.

Keynote address, HiPC Symposium on High Performance Computer Architecture, Goa, India, December 2007. Title: The Transformation Hierarchy in the Era of Multi-Core.

Keynote address, 25th International Conference on Computer Aided Design (ICCD), Squaw Valley, October 2007. Title: Microprocessor Performance, Phase II: Harnessing the Transformation Hierarchy.

Keynote address, Second Spanish Conference on Informatics (CEDI 2007), Zaragoza, September, 2007. Title: The Microprocessor Ten Years from Now: Why it is Relevant to all Informatics.

Keynote address, 16th International Conference on Parallel Architecture and Compiling Techiques (PACT), Brasov, Romania, September 2007. Title: Harnessing the Transformation Hierarchy.

Keynote address, Workshop on Computer Architecture Education (WCAE 2007), in conjunction with ISCA, San Diego, June, 2007. Title: LC-3, x86, or ??: The First ISA for Students to Study.

Keynote address, Student Congress, Durango, Mexico, September 2006.

Keynote address, 33rd Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), Boston, June, 2006. Title: Computer Architecture Research and Future Microprocessors: Where do we go from here?

Keynote address, 2006 Spring convention of the State of New Jersey High School Science and Math Teachers, Newark, March, 2006. Title: Education: Some thoughts after 35 years in the trenches.

Keynote address, 4th Annual Dalhousie Computer Science In-House Conference, Halifax, Nova Scotia, September, 2005. Title: The Microprocessor: Its Characteristics Ten Years from Now.

Keynote address, 4th annual Encuentro Estudiantil (National ACM Congress of Mexican Computer Science Students), Puebla, March, 2005. Title: Are there any questions?

Keynote address, 3rd IEEE/ACS International Conference on Computer and System Applications (AICCSA-05), Cairo, Egypt, January, 2005. Title: The Microprocessor of the Year 2014: Do Pentium 4, Pentium M, and Power 5

provide any hints?

Keynote address, 16th Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Foz du Iguazu, Brazil, October, 2004. Title: The Microprocessor of the Year 2014: Do Pentium 4, Pentium M, and Power 5 provide any hints?

Plenary address, XXIX Pan-American Engineering Symposium, Mexico City, September, 2004. Title: Future Trends in Computer Architecture.

Plenary address, 2004 International Supercomputer Conference, Heidelberg, June, 2004. Title: "The processor in 2014: What are the challenges, how do we meet them?"

Keynote address, 2004 IEEE International Symposium on Performance Analysis of Systems and Software, Austin, March, 2004. Title: Performance Analysis: A big plus, or an even bigger minus.

Keynote address, 10th annual IEEE International Symposium on High Performance Computer Architecture (HPCA-10), Madrid, Spain, February, 2004. Title: Microarchitecture: Are we finally done?

Keynote address, HiPC 2003, Hyderabad, India, December, 2003. Title: The High Performance Microprocessor in the Year 2013: What will it look like? What it won't look like?

Keynote address, International Conference on Information Technology (CIT), Bhubaneswar, India, December, 2003. Title: Current bottlenecks to continued high performance microprocessors, and what we can do to get passed them.

Keynote address, SSGRR 2003s, L'Aquila, Italy, July, 2003. Title: A Microarchitect's perspective: What computer technology will provide and won't provide by the year 2020.

Keynote address, Computer Architecture Education Workshop, International Symposium on Computer Architecture (ISCA), June, 2003. Title: Teaching and Teaching Computer Architecture: Two Very different topics (Some Opinions about each).

Keynote address, 2nd annual Encuentro Estudiantil (National ACM Congress of Mexican Computer Science Students), Guanajuato, May, 2003. Title: What is Moore's Law REALLY all about?

Keynote address, ICCD, Austin, TX, September, 2001. Title: There is still plenty of work that needs to get done.

Keynote address, 26th EuroMicro Congress, Maastricht, Netherlands, September, 2000. Title: Higher and Higher Performance Microprocessors: Are the Problems Just too Hard to Solve?

Plenary address, EuroPar-2000, Munich, Germany, August, 2000. Title: Despite the Nay-Sayers to the Contrary, Moore's Law is Alive and Well and Still Providing Opportunities.

Keynote address, Seventh International Conference on Advanced Computing, Roorkee, India, December, 1999.

Keynote address, International Symposium on New Trends in Computer Architecture, Gent, Belgium, December, 1999.

Keynote address, 11th Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Natal, Brazil, September, 1999.

Keynote address, Workshop on Workload Characterization, 31st Annual Symposium on Microarchitecture, Dallas, TX, November 1998.

Keynote address, Workshop on Simultaneous Multithreading, 4th Annual High Performance Computer Architecture Conference (HPCA-4), Las Vegas, January, 1998.

Keynote address, Computer Architecture Education Workshop, 4th Annual High Performance Computer Architecture Conference (HPCA-4), Las Vegas, January, 1998. Title: High Tech -- The Enemy of Education?

Keynote address, IEEE/ACM 11th Annual International Supercomputer Conference, Vienna, July, 1997.

Keynote address, IEEE International Performance Conference on Computers and Communications, Phoenix, Arizona, February, 1997.

Keynote address, IBM Conference on Performance Analysis and its Influence on Computer Design, Austin, March 27, 1996.

Plenary address, 29th Annual Hawaii International Conference on System Sciences, Maui, January, 1996. Title: The Microprocessor and its Performance in the Year 2000.

Plenary address, ACM/IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT95), Limassol, Cyprus, June, 1995.

Keynote address, International Congress on Massively Parallel Information Systems, Ischia, Italy, May, 1994.

Keynote address, International Federation of Information Processing (IFIP) Working Conference on Architectures and Compilation Techniques for Fine and Medium Grain Parallelism, Orlando, Florida, January, 1993. Title: The Compiler and the Microarchitecture: Partners, not Adversaries.

Keynote address, 25th Annual IEEE/ACM International Symposium and Workshop on Microarchitecture, Portland, OR, November, 1992.

Keynote address, Euromicro Congress 1992, Paris, September, 1992.

Plenary address, 25th Annual Hawaii International Conference on System Sciences, Kauai, January, 1992. Title: What do we do about the Speed of Light?

Keynote address, 5th International Congress on Computer Architecture and Performance Modeling, Torino, Italy, February, 1991. Title: "Computer Architecture and Performance Modeling, Obtaining Meaningful Information."

Keynote address, NCR Corporation Workshop in Performance Measurement, Cambridge, OH, December, 1988. Title: "The light is better over here."

Keynote address on "Computer Architectures for Artificial Intelligence," IEEE 1987 Symposium on Artificial Intelligence: Applications in Engineering, Minneapolis, Minnesota, January, 1987.

Keynote address (Architecture) at the annual Livermore-Los Alamos invited Salishan Workshop on "Toward a Science of Parallel Computation," March, 1986.

DISTINGUISHED LECTURES

Lecturer, Severo Ochoa Memorial Lecture Series, Barcelona Supercomputer Center, June, 2018. "Title: Deep Learning and Quantum Computing; Is anything else worth working on?"

Lecturer, UC Irvine Distinguished Lecture, Systems, March, 2017. Title: Processor Paradigms: Evolution or Disruption and the importance of the Transformation Hierarchy Moving Forward.

Lecturer, ETH Distinguished Colloquium Series, Zurich, Switzerland, November, 2016. Title: Continuing to Ride the Performance Wave -- Even if Moore's Law Comes to an End.

Lecturer, UC Riverside Distinguished Lecture Series, Riverside, CA, October, 2015. Title: The END of X, the BEGINNING of Y.

Lecturer, Michigan Technological University Distinguished Lecture Series, Houghton, MI, September, 2015. Title: The END of X, the BEGINNING of Y.

Lecturer, Michigan Technological University Distinguished Lecture Series, Houghton, MI, September, 2015. Title: The CORRECT first course in computing for serious students.

Lecturer, Severo Ochoa Memorial Lecture Series, Barcelona Supercomputer Center, June, 2015. Title: The Von Neumann Architecture and Moore's Law: What are the Implications moving forward.

Lecturer, ECE Distinguished Lecture Series, Northeastern University, March, 2015. Title: The End of Von Neumann, the End of Moore's Law: What will the Microprocessor of 2015 look like?

Lecturer, University of Southern California Energy Informatics Distinguished Seminar Series, February, 2015. Title: Parallelism: A serious goal or a silly mantra (...and what about the end of the Von Neumann architecture)

Lecturer, Severo Ochoa Memorial Lecture Series, Barcelona Supercomputer Center, July, 2014. Title: Parallelism: a serious goal or a silly mantra (and what else is needed for the microprocessor of 2024)

Lecturer, Texas A&M Distinguished Lecture Series, May, 2014. Title: The correct FIRST course for serious students of computing.

Lecturer, Texas A&M Distinguished Lecture Series, May, 2014. Title: Parallelism: A serious goal or a silly mantra (...and what else is needed for the Microprocessor of 2024).

Lecturer, UT Austin Distinguished Lecture Series, September, 2013. Title: The Microprocessor: How we got to where we are. Why are things different now? Where do we go from here?

Inaugural lecturer, Henry Taub Memorial Distinguished Lecture Series, Technion, Haifa, Israel, June, 2013. Title: The Microprocessor: Where we've been, Where we are heading, and What we have to do differently moving forward.

Lecturer, Northwestern University Distinguished Speakers Series, April, 2011. Title: The Design of Future Microprocessors: The User Interface has important implications.

Lecturer, Chalmers University Distinguished Speaker Colloquium Series, September, 2010. Title: Future High Performance Microprocessors: What will they look like? How will we get there?

Lecturer, UIUC Parallel@Illinois Distinguished Lecture Series, April, 2010. Title: Future Microprocessors: Multicore, Mega-nonsense, and What We Must Do Differently Moving Forward.

Lecturer, Texas A&M CSE Distinguished Lecturer Series, March, 2010. Title: High Performance Microprocessors ten years from now: What are the problems? How do we solve them?

Lecturer, The HiPEAC/European Union Task force on Undergraduate Education, Pisa, January, 2010. Title: The Art of Teaching.

Lecturer, The HiPEAC/European Union Task force on Undergraduate Education, Pisa, January, 2010. Title: The bottom-up approach to teaching introductory computer architecture and programming.

Lecturer, Carnegie-Mellon Distinguished Lecture Series, October, 2009. Title: Future Microprocessors: Multi-core, Multi-nonsense, and What We Must Do Differently Moving Forward.

Lecturer, Rice University VISEN Distinguished Lecture Series, April, 2009. Title: The Challenges of Multicore: Information and Mis-Information

Lecturer, University of Texas at Arlington Distinguished Lectures Series, December, 2008. Title: Education: Are there any questions?"

Lecturer, Pennsylvania State University Distinguished Lectures Series, April, 2007. Title: The Fundamentals: Vehicle to the Year 2017- Tomorrow's Graduates, Tomorrow's Microprocessors

Lecturer, The University of Arizona Distinguished Lectures Series, February, 2007. Title: The Microprocessor Ten Years from Now: What are the Challenges? What can we do about them?

Lecturer, The European Union's 2nd Annual HiPEAC Summer School for PhD students, July, 2006, L'Aquila, Italy. Five 90 minute lectures on the subject, Advanced Microarchitecture.

The Saul Gorn Memorial Lecturer, University of Pennsylvania, April, 2006. Title: Computer Architecture Research: Is it Dead? Is it in need of Revitalization? Where do we go from here?

Lecturer, The University of Nebraska Distinguished Lecturer Series, April, 2006. Title: The Microprocessor Ten Years from Now.

Lecturer, The Northeastern University Distinguished Lecturer Series, April, 2006. Title: Future Microprocessors, where do we go from here?

The Irons Distinguished Lecturer, Rutgers University, March, 2006. Title: Future Microprocessors, where do we go from here?

Lecturer, The European Union's Inaugural HiPEAC Summer School for PhD students, July, 2005, L'Aquila, Italy. Five 90 minute lectures (Monday through Friday) on the subject Advanced Microarchitecture.

Lecturer, Distinguished Lecturer Series, SMU, April, 2005. Title: "The Microprocessor in the Year 2015: Issues, Challenges, Potential Avenues to Solutions."

Lecturer, ISTeC Distinguished Lecturer Series, Colorado State University, Ft. Collins April, 2005. Title: "Education. Are there any questions?"

Lecturer, Distinguished Lecturer Series, Computer Science Dept, Purdue University, March 2005. "Are there any questions?"

Lecturer, Distinguished Lecturer Series, Rice University, Houston, TX, November, 2004. Title: Trends in Computer Architecture.

Lecturer, Distinguished Lecturer Series, Courant Institute, New York University, October, 2004. Title: The Microprocessor of the Year 2014: Do Pentium 4, Pentium M, and Power 5 provide any hints?

Lecturer, Distinguished Lecturer Series, Carnegie Mellon University, Pittsburgh, April, 2004. Title: "The Microprocessor Ten Years from now: What are the challenges, how do we meet them?"

Lecturer, City University of Hong Kong Distinguished Lecture Series on Teaching and Learning, Hong Kong, January, 2004. Title: Ten Commandments of Good Teaching.

Lecturer, Distinguished Lecture Series, University of California, Irvine, December, 2003. Title: "Fundamentals: Moore's Law, Microarchitecture, and the Microprocessor of the year 2014."

Lecturer, Worcester Polytechnic Institute Distinguished Lecturer Series, September, 2003. Title: The High Performance Microprocessor in the Year 2013: Will the laws of Physics finally catch up with the Microprocessor development cycle?"

Lecturer, The University of Texas ECEntury Distinguished Lecturer Series, March, 2003.

Robert T. Chien Memorial Lecture, University of Illinois, Urbana-Champaign, December, 2002.

Lecturer, the Harvard University Distinguished Lecture Series, October, 2002. "The Correct Way to Introduce Students to Computers."

Lecturer, The Erik Jonsson School of Engineering Distinguished Lecture Series, The University of Texas at Dallas, October, 2002.

Lecturer, University of Alberta Distinguished Lecturer Series in Electrical Engineering, October, 2002.

Lecturer, California State University at Fresno Distinguished Lecture Series in Computer Engineering, May, 2002.

The 2001-2002 Distinguished Lecturer in Computer Science, University of Wisconsin, La Crosse, April, 2002.

Lecturer, Georgia Tech Distinguished Lecturer Series in Computer Engineering, April, 2002.

The William Mong Distinguished Lecturer at the University of Hong Kong, March, 2002.

Lecturer, University of Illinois Distinguished Lecturer Series in Computer Science, February, 2002.

Lecturer, University of Pittsburgh Distinguished Lecturer Series, October, 2001.

The Birck Distinguished Lecturer, Purdue University Distinguished Lecture Series, March, 2001.

Lecturer, University of California, Riverside Distinguished Lecturer Series, January, 2001.

Lecturer, Colorado State University Distinguished Lecturer Series, April, 2000.

Lecturer, University of Delaware Distinguished Lecturer Series, March, 2000.

Lecturer, Texas A&M University Distinguished Lecturer Series, February, 2000.

Invited lecturer, HP2EUR Conference, Tromso, Norway, June, 1999.

Lecturer, Carnegie-Mellon University Distinguished Lecturer Series, April, 1998.

Lecturer, University of Southern California Distinguished Lecturer Series, February, 1998.

Lecturer, UCLA Distinguished Lecturer Series, November, 1996.

Lecturer, University of Southwestern Louisiana Distinguished Lecturer Series, November, 1996.

Lecturer, University of Texas, Austin Distinguished Lecturer Series, November, 1996.

Lecturer, Texas A&M University Shell Oil Distinguished Lecturer Series, February, 1996.

Distinguished lecturer, Taiwan Government. Series of three lectures, May 4,5, 1995. At ITRI, May 4: "HPS, The Microarchitecture for High Performance Processors." At Chiao Tung University, May 4: "The Next Challenge: a 10 IPC Processor." At National Taiwan University, May 5: "Branch Prediction: After Yeh's Algorithm, What?"

Invited lecturer, "Doctoral Network," a one-week summer school for leading PhD students in computer architecture, organized by the French National Education Administration, July, 1994.

Lecturer, Northwestern University Distinguished Lecturer Series, May, 1994.

Inaugural lecturer, the IEEE Distinguished Visitor Program for Asia and the Pacific. Lectures were presented in Bombay, Calcutta, Delhi, and Hong Kong, May 1993.

Lecturer, University of California, San Diego Distinguished Lecturer Series, April, 1992.

Lecturer, University of Maryland Distinguished Lecturer Series, November, 1991.

Distinguished Speaker, 1991 IEEE Joint Technical Committees Meeting, Rochester, New York, March 1991. Title: "Computer Architecture Choices.

Lecturer, Case-Western Reserve University Distinguished Lecturer Series, December, 1989.

Lecturer, Northeastern University Distinguished Lecturer Series, May, 1989.

Lecturer, Clemson University NCR Distinguished Lecturer Series, March, 1989.

At the invitation of the Ministry of Education of the Italian government, a series of 16 lectures on Advanced Concepts in Computer Architecture at the University of Pavia, May, 1985.

National Distinguished Visitor of the IEEE, 1989-93.

National ACM Lecturer: 1975-76, 1985-92, 1995-present.

OTHER NOTABLE TALKS

Invited talk, PER2018, Gothenburg, Sweden, May, 2018. Title: "Old Paradigms, New Instances, and their influence on the future."

Invited vision talk, Stamatis Symposium: Celebrating the Life of Stamatis Vassiliadis, Samos, July 2017. Title: "Economics be damned!"

Invited Global Lecture, Zhejiang University, on occasion of their 120th anniversary celebration, May 22, 2017. Title: "The end of Moore's Law: an obstacle to discourage or an opportunity to embrace"

Invited talk, 1st Technion Computer Engineering Conference (TCE), Haifa, June, 2011. Title: "Future Microprocessors: The User Interface has Important Implications."

Invited talk, panel on "Microelectronics: The Beginning of the End or the End of the Beginning," 2011 Annual Conference of The Academy of Medicine, Engineering and Science of Texas, January 6, 2011, Austin, TX.

Invited speaker, 50th Anniversary Celebration of the first computer installed in Mexico, organized by the Commission on Science and Technology of the LX Legislature, Federal Government of Mexico, Camera de Diputados, Mexico City, September 3, 2008. Title: "Future Microprocessors and their implications for Computer Science Education in Mexico."

Invited speaker, "eContent Summit: Scenarios for the future," a workshop organized by the President of Croatia, Brijuni, September, 2007. Title: eContent: Static vs. Dynamic; In Education, it makes a huge difference.

Featured speaker, IEEE Computer Society 60th Anniversary Celebration, Hotel Intercontinental, San Juan, Puerto Rico, June, 2006. Title: The Future of Computer * (Are we in Serious Trouble?).

Banquet address, 19th IEEE International Parallel & Distributed Processing Symposium, Denver, April, 2005. Title: A Unifying Theory of Distributed Processing.

Interview on "Newsmakers," WLSU Radio, La Crosse Wisconsin, on the future of computer technology. Aired May 6, 2002.

Interview on "Generation.e," CNBC Asia, on the topic, "The future capabilities of microprocessors," March 8, 2002.

INVITED PANELS at INTERNATIONAL CONFERENCES, SYMPOSIA

Member, invited panel (in the form of a loosely structured debate) at the 47th annual IEEE/ACM International Symposium on Microarchitecture, Cambridge, England, December 2014, on the topic, "The Von Neumann Architecture is Dead."

Member, invited panel at 37th annual IEEE/ACM International Symposium on Computer Architecture, Saint-Malo, June 2010, on the topic, "Computer Architecture is Dead, Long Live Computer Architecture."

Member, invited panel at HiPEAC 2010, January, 2010, on the topic: "Heterogenous vs. Homogenous Computing."

Member, invited panel at IEEE International Symposium on Workload Characterization, Austin, October, 2009, on the topic:"What's the new General Purpose?"

Chair, invited panel at 35th annual IEEE/ACM International Symposium on Computer Architecture, Beijing, June, 2008, on the topic, "Computer Architecture Research and ISCA, Have we lost our compass?"

Member, invited panel at 40th annual IEEE/ACM International Symposium on Microarchitecture, Chicago, December, 2007, on the topic, "Computing Beyond Von Neumann."

Member, invited panel at the 13th annual IEEE International High Performance Computer Architecture Symposium, Phoenix, February, 2007, on the topic, "Researching Novel Systems: To Instantiate, Emulate, Simulate, or Analyticate?"

Member, invited panel at the 39th IEEE/ACM International Symposium on Microarchitecture, Orlando, Florida, December, 2006, on the topic, "The Implications of Nanotechnology."

Member, invited panel at the 12th annual IEEE International High Performance Computer Architecture Symposium, Austin, February, 2006, on the topic, "Patenting the Fruits of Academic Research: What are the Implications?"

Moderator, invited panel at 16th Symposium on Computer Architecture and High Performance Computing, Foz do Iguacu, Brazil, October, 2004.

Member, invited panel at 2004 IEEE International Symposium on Performance Analysis of Sytems and Software, Austin, March, 2004, on the topic, "The Future of Simulation: A Field of Dreams?"

Member, invited panel at the 10th annual IEEE International High Performance Computer Architecture Symposium, Madrid, February, 2004, on the topic, "Bridging the Research Gap between Academia and Industry."

Member, invited panel at the 8th annual IEEE International High Performance Computer Architecture Symposium, Boston, February, 2002, on the topic, "Processors, Memory, Interconnect, where will the greatest benefit come from in the next ten years."

Member, invited panel at the 34th annual IEEE/ACM International Symposium on Microarchitecture, Austin, TX, December, 2001, on the topic, "Intellectual Property: Microarchitecture is in the thick of it."

Member, invited panel at IEEE ICCD Symposium, Austin, September, 2001.

Member, invited panel at the 30th annual IEEE/ACM International Symposium on Microarchitecture, Raleigh, NC, December, 1997 on the topic, "The future of ISAs other than x86."

Member, invited panel at the 28th annual IEEE/ACM International Symposium on Microarchitecture, Ann Arbor, December 1995, on the topic, "Single-chip performance on the Microprocessor of the year 2000."

Moderator, invited panel at the 21th annual IEEE/ACM International Symposium on Computer Architecture, Chicago, April 1994, on the topic, "Computer Architecture as a Discipline in the year 2000."

Moderator, invited panel at the 20th annual IEEE/ACM International Symposium on Computer Architecture, San Diego, May 1993, on the topic, "Experimental Research: How do we Measure Success."

Member, invited panel at the 19th annual IEEE/ACM International Symposium on Computer Architecture, Australia, May 1992, on the topic, "Processor architectures for Peta-op Performance."

Member, invited panel at the 18th annual IEEE/ACM International Symposium on Computer Architecture, Toronto, May 1991, on the topic, "The Influence of University Research in Computer Architecture on the development of new commercial computers."

Member, invited panel at the 17th annual IEEE/ACM International Symposium on Computer Architecture, Seattle, May 1990, on the topic, "Better than one operation per clock: Vectors, VLIW, and Superscalar."

Member, invited panel at the 13th annual IEEE/ACM International Symposium on Computer Architecture, Tokyo, June 1986, on the topic, "AI Machines and Scientific Machines, Are they compatible?"

EDITORSHIPS

Associate Editor, *Computer Architecture Letters*, 2006-2010.

(Founding) Editor-in-Chief, *Computer Architecture Letters*, 2001-2005.

Member, Editorial Board, *Proceedings of the IEEE,* 1996-2000.

Associate Editor of the *IEEE Transactions on Computers*, 1992-1996.

Member, Editorial Board, *IEEE Computer*, 1989-1992.

Guest Co-Editor, *IEEE Micro* Top Picks Special Issue, January/February, 2011.

Guest Editor of a Special Issue of *IEEE Computer* (December, 1997) on the topic, Strategic Directions for Computer Architecture Research.

Guest Editor of a Special Issue of *Proceedings of the IEEE* (December, 1995) on the topic, Microprocessors.

Guest Editor of a Special Issue of *IEEE Computer* (March, 1994) on the topic, The I/O Subsystem, A Candidate for Improvement.

Guest Editor of a Special Issue of *IEEE Computer* (January, 1991) on the topic, Experimental Research in Computer Architecture and Performance Measurement.

Guest Editor of a Special Issue of *IEEE Computer* (January, 1989) on the topic, Design and Engineering Tradeoffs in the Implementation of Various Commercially Successful Computers.

EXTERNAL EXAMINING BOARDS

External Examiner, Graduate program in Computer Science and Engineering, UC Riverside, November, 2015.

External Examiner, Graduate program in Electrical Engineering and Computer Engineering, University of Cincinnati, October, 2005.

External Examiner, Computer Engineering Research, National Foundation for Science and Technology, Lisbon, Portugal, January, 2005.

External Examiner, Electrical and Computer Engineering Department, Northwestern University, May, 2001.

External Examiner, Computer Science Department, UNLV, March, 2001.

External Examiner, Texas A&M PhD program in Electrical and Computer Engineering, March, 2000.

External Examiner, Computer Engineering Research, National Foundation for Science and Technology, Lisbon, Portugal, December, 1999.

External Examiner, City University of Hong Kong, Computer Science Department, 1996-2003.

Member, Dean's External Advisory Committee, School of Electrical Engineering and Computer Science, Polytechnic University of New York, 1992-1994.

PROFESSONAL SERVICE

Member of the Board of Governors of the IEEE Computer Society, 1989-1993.

Vice President for Press Activities of the IEEE Computer Society, 1992.

General Co-Chairman, International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC-2010), Pisa, January, 2010.

General Co-Chairman, 12th International Symposium on High Performance Computer Architecture, Austin, TX, February, 2006.

General Chairman, 29th International IEEE/ACM Symposium on Computer Architecture (ISCA), Anchorage, May, 2002.

General Chairman, 34th International IEEE/ACM Workshop and Symposium on Microarchitecture, Austin, TX, November, 2001.

General Chairman, 21st International IEEE/ACM Workshop on Microarchitecture and Microprogramming, San Diego, CA, November, 1988.

General Chairman, First International Symposium on High Performance Computer Architecture, Raleigh, NC, January, 1995.

Program Co-Chairman, 15th International IEEE/ACM Symposium on Computer Architecture (ISCA), June, 1988.

Program Co-Chairman (Computer Architecture), IEEE/ACM International Conference on Supercomputing, Melbourne, July, 1998.

Member of the Advisory Committee, ACM Distinguished Lectureship Program, 1998-2003; Director, 2001-2002.

Chairman, Joint ACM-IEEE Computer Society Eckert-Mauchly Award Committee, 1992, 1999. Member of the committee, 1988-1992, 1998-2000, 2012-2014.

Member, IEEE Computer Society Harry Goode Award Committee, 2001-2010, Chair, 2004-2006.

Member, IEEE Computer Society Wallace W. McDowell Award Committee, 2001-2010, Chair, 2004-2006.

Member, IEEE Computer Society B. Ramakrishnan Rau Award Committee, 2012, 2015.

Chairman of a Task Force appointed by the President-elect of the IEEE Computer Society to investigate problems dealing with the education of computer engineers and computer scientists, starting with high school preparation, continuing with educational programs in the Colleges, and finally dealing with continuing education beyond graduation, July, 1991.

Member of the Strategic Planning Committee of the IEEE Computer Society, 1991.

Member, IEEE Computer Society Taylor Booth Award Committee, 1993-1996.

Member, Educational Activities Board, IEEE Computer Society, 1988-1994.

Invited participant (one of 20), NSF Workshop on Grand Challenges in Computer Architecture for the Support of High Performance Computing, Purdue University, December 1991. A report of that workshop appeared as an invited paper (with 20 co-authors) in the Journal of Parallel and Distributed Computing. High Performance Architectures for Numerical and Symbolic Computations, University of California, Berkeley, February 13-15, 1985.

Member, Steering Committee of the 19th, 21st, 22nd, 23rd, 24th, 25th, 26th, 28th, 29th, 30th and 31st, 33rd, 35th, 36th, 38th, 39th, 40th, and 41st International Symposia on Computer Architecture, May, 1989, April, 1994, June, 1995, May, 1996, June, 1997, June, 1998, May, 1999, May, 2001, May, 2002, June, 2003, June, 2004, June, 2006, June, 2008, and June, 2009, June, 2011, June, 2012, June, 2013, June, 2014.

Member, Steering Committee of the 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, 41st, 42nd, 43rd, 44th, 45th, 46th, 47th, 48th, 49th, 50th International Symposium on Microarchitecture, December, 1992, December, 1993, December, 1994, December, 1995, December, 1996, December, 1997, December, 1998, November, 1999, December, 2000, December, 2001, November, 2002, December, 2003, December, 2004, November, 2005, December, 2006, December, 2007, November, 2008, December, 2009, December, 2010, December, 2011, December, 2012, December, 2013, December, 2014. December, 2015, October, 2016, October, 2017.

Member, Steering Committee of the 2nd, 3rd, 4th, 5th, 6th, 7th, 8th, 9th, 10th, 11th, 12th, 13th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st IEEE International Symposium on High Performance Computer Architecture, San Jose, February, 1996, San Antonio, February, 1997, San Francisco, February, 1998, Orlando, January, 1999, Toulouse, January, 2000, Monterrey, Mexico, January, 2001, Boston, January, 2002, Anaheim, January, 2003, Madrid, February, 2004, San Francisco, February, 2005, Austin, February, 2006, Phoenix, February, 2007, Salt Lake City, February 2008, Raleigh, February 2009, Bangalore, January 2010, San Antonio, February 2011, New Orleans, February, 2012, Shenzhen, China, February, 2013, Orlando, Florida, February, 2014, February, 2015.

Member, Steering Committee, 23rd, 24th IEEE/ACM International Symposium on Parallel Architectures and Compilation Techniques, Edmunton, August, 2014, San Francisco, October, 2015.

Member, Steering Committee, HiPEAC-2011, Iraklion, Crete, January, 2011.

Member, Technical Advisory Board, IEEE Technical Committee on Computer Architecture, 1995-2014.

Organizer/co-ordinator, minitrack on the subject: "Real Machines: Design Choices, Engineering Trade-offs," at the 20th Hawaii International Conference on Systems Science, January, 1989.

Organizer/co-ordinator, minitrack on the subject: "Experimental Research in Computer Architecture," at the 21st Hawaii International Conference on Systems Science, January, 1990.

Organizer/co-ordinator, second consecutive minitrack on the subject: "Experimental Research in Computer Architecture," at the 22nd Hawaii International Conference on Systems Science, January, 1991.

Organizer/co-ordinator, minitrack on the subject: "I/O Architecture: Issues and Bottlenecks," at the 23rd Hawaii International Conference on Systems Science, January, 1992.

Organizer/co-ordinator, second consecutive minitrack on the subject: "I/O Architecture: Issues and Bottlenecks," at the 24th Hawaii International Conference on Systems Science, January, 1993.

Lecturer, IEEE Computer Society's Tutorial Program on the subject, "Computer Architecture Choices."

Lecturer, IEEE Computer Society's one-day tutorial for High School Math and Science teachers, 1991-94.

External reviewer, Research Programs Review at the Lawrence Livermore National Laboratory, December, 1984.

Member, organizing committee for the First Northern California Universities Supercomputer Workshop, Lawrence Livermore National Laboratory, February, 1984.

Member, Program Committee for more than 50 conferences and symposia, including the 31th International Workshop on Microarchitecture and Microprogramming (Dallas, December 1998), the 1998 3rd International conference on Parallel Architectures and Compiling Techniques (Paris, October, 1998), the 5th International High Performance Computer Architecture Conference (Orlando, January, 1999), 32th International Symposium on Microarchitecture (Haifa, November, 1999), HPCA-7 (Monterrey, January, 2001), ISCA-2001 (Goteborg, June, 2001), 8th International Conference on High Performance Computing (Hyderabad, December, 2001), and ICS (New York City, June, 2002), ISCA-2004 (Munich, June 2004), Micro-37 (San Francisco, Dec 2004), HiPEAC (Barcelona, Nov 2005), Micro-38 (Barcelona, Nov 2005), ISCA (Boston, 2006), Micro-39 (Orlando, 2006), HPCA-13 (Phoenix, 2007), Micro-40 (Chicago, 2007), HPCA-14 (Salt Lake City, 2008), ISCA (Beijing, 2008), SBAC-PAD (Brazil, 2008), Micro-41 (Como, 2008), HPCA-15 (Raleigh, 2009), SBAC-PAD (Sao Paolo, 2009), HPCA-16 (Bangalore, 2010), SBAC-PAD (Rio, 2010), ISCA (San Jose, CA, 2011), Micro-44 (Porto Alegre, 2011), Micro-45 (Vancouver, 2012), ICS (2014), SBAC-PAD (Paris, 2014).

Reviewer, NSF proposals, ACM and IEEE journals and conferences.

Accreditation visitor, ABET (computer engineering) 1990-1994.

Accreditation visitor, CSAB (computer science), 1986-1992.

Chairman, Curriculum Assistance Committee of the IEEE Computer Society, 1978-1981. In this capacity I organized and conducted workshops dealing with the Model Curriculum in Computer science and Engineering in 1979 (San Francisco), 1980 (Chicago) and 1981 (Washington, D.C.).

General Chairman, 5th Annual Southeastern Symposium on System Theory, Co-hosted by N.C. State, UNC-Chapel Hill, Duke, March, 1973.

Member, Steering Committee, COINS-3, 1969.

Program Chairman, 1975 Southeastern Regional ACM Meeting, April, 1975.

Session Chairman, more than 50 conferences, including: COINS-3 (January, 1969), Hawaii International Conference on Systems Sciences (January, 1970), 6th Annual Southeastern Systems Theory Symposium (1974), 4th International Multi-valued Logic Symposium (1974), 7th Annual Southeastern Systems Theory Symposium (1975), Fall Compcon (September, 1981), Spring Compcon (February, 1983), Spring Compcon (February, 1984), Micro-17 (October, 1984), Spring Compcon (February, 1985), Micro-18 (December, 1985), HICSS-19 (January, 1986), Spring Compcon (March, 1986), 13th ICAC (June, 1986), Micro-19 (October, 1986), Micro-20 (December, 1987), Compcon 88 (March, 1988), Micro-21 (December, 1988), Compcon 89 (February, 1989), International Supercomputing Conference (June, 1989), HICSS-1991 (January, 1991), Micro-24 (November, 1991), ISCA-13 (June, 1986), HICSS-1992 (January, 1992), ISCA-19 (May, 1992), Micro-25 (November, 1992), IFIP Workshop on Architecture and Compiling (January, 1993), HICSS-1993 (January, 1993), Micro-26 (December, 1993), IPPS (April, 1994), Micro-27 (December, 1994), HPCA-1 (January, 1995), ISCA (June, 1995), PACT (June, 1995), Micro-28 (December, 1995), ICS (July, 1997), Micro-30 (December, 1997), HPCA-5 (January, 1999), PACT (October, 1999), ISCA (June, 2004), ISCA (June, 2006), HPCA (February, 2008), HPCA (January, 2010).

TUTORIALS (Sponsored by the professional computer societies, IEEE_CS and ACM)

Instructor, one day tutorial on current hot topics in Computer Architecture, as follows: IEEE Tutorial Week West, October 1, 1984, IEEE Tutorial Week West, June 7, 1985, IEEE Compcon 86, March 1, 1986, Compcon 88, February 29, 1988, Compcon 89, February 27, 1989, Compcon 90, February 26, 1990, Compcon 91, February 25, 1991, Compcon 92, February 24, 1992, Compcon 93, February 22, 1993, Compcon 94, February 28, 1994, Compcon 95, March 5, 1995, Supercomputing 95, December 4, 1995, Compcon 96, February 25, 1996, Compcon 97, February 23, 1997, Supercomputing 2001, November 11, 2001.

Instructor, half-day tutorial on architectural mechanisms for exploiting concurrency, as follows: 17th IEEE/ACM International Symposium on Computer Architecture, May 28, 1990, 18th IEEE/ACM International Symposium on Computer Architecture, May 27, 1991, 19th IEEE/ACM International Symposium on Computer Architecture, May

17, 1992, International Conference on Parallel Processing, August 17, 1992, 21st IEEE/ACM International Symposium on Computer Architecture, April 19, 1994, 1994 International Conference on Parallel Architectures and Compiler Technology, August 23, 1994, 22nd IEEE/ACM International Symposium on Computer Architecture, June 21, 1995, the 1995 International Conference on Parallel Architectures and Compiler Techniques, June 27, 1995, the 23rd IEEE/ACM International Symposium on Computer Architecture, May 21, 1996, IEEE Hot Chips Symposium, August 18, 1996, and ICCD, October 7, 1996.

Instructor, one-day tutorial to non-Computer-Architects on the state-of-the-art in Computer Architecture, as follows: 26th Annual HICSS Conference, January 5, 1993, 27th Annual HICSS Conference, January 4, 1994, 28th Annual HICSS Conference, January 3, 1995, 29th Annual HICSS Conference, January 2, 1996.

Instructor, one-day tutorial on Microarchitecture: Concepts, Tradeoffs, the Future, PACT 2007, Brasov, Romania, September, 2007.

BOOKS

Introduction to Computing Systems: from bits and gates to C and beyond, McGraw-Hill, 2001 (ISBN No. 0-07-237690-2), co-authored with Professor Sanjay Jeram Patel. 2nd edition, McGraw-Hill, 2004 (ISBN No. 0-07-246750-9, ISBN 0-07-121503-4(ISE)).

MAGAZINE/NEWSLETTER ARTICLES

Retrospective on the Two-Level Adaptive Branch Predictor paper, Micro Test of Time Award (with Tse-Yu Yeh), in Common Bonds: MIPS, HPS, Two-Level Branch Prediction, and Compressed Code RISC, *IEEE Micro*, July/August, 2016.

Retrospective on the three HPS Papers, Micro Test of Time Awards (with Wen-mei Hwu, Michael Shebanow and Stephen Melvin, in Common Bonds: MIPS, HPS, Two-Level Branch Prediction, and Compressed Code RISC, *IEEE Micro*, July/August, 2016.

An Interview with Yale Patt, *Communications of the ACM*, June, 2016 [the full interview is available at https://vimeo.com/166395724.

Data Marshaling for Multi-core Architectures, *IEEE Micro*, Top Picks Special Issue, January/February, 2011. [earlier version in *Proceedings of ISCA 2010*, Saint-Malo, France, June 2010] (with M. Aater Suleman, Onur Mutlu, Jose Joao, and Khubaib).

Accelerating Critical Section Execution with Asymmetric Multi-Core Architectures, *IEEE Micro*, Top Picks Special Issue, January/February, 2010. [earlier version in *Proceedings of ASPLOS XIV,* Washington D.C., March 2009] (with Aater Suleman, Onur Mutlu, and Moinuddin Qureshi).

Adaptive Insertion Policies for High-Performance Caching, *IEEE Micro*, Top Picks Special Issue, January/February, 2008. [earlier version in *Proceedings, 34th annual IEEE/ACM International Symposium on Computer Architecture*, San Diego, CA, June 2008 (with Moinuddin K. Qureshi, Aamer Jaleel, Simon C. Steely Jr., and Joel Emer).

Single-Threaded vs. Multithreaded: Where Should We Focus? *IEEE Micro*, November 2007. (with Joel Emer, Mark D. Hill, Joshua J. Yi, Derek Chiou, and Resit Sendag).

Diverge-Merge Processor: Generalized and Energy-Efficient Dynamic Predication, *IEEE Micro*, Top Picks Special Issue, January/February, 2007. [earlier version in *Proceedings, 39th annual IEEE/ACM International Symposium on Microarchitecture*, Orlando, Florida, December, 2006] (with Hyesoon Kim, Jose Joao, and Onur Mutlu)..XP Techniques for Efficient Processing in Runahead Execution Engines. *IEEE Micro*, Top Picks Special Issue, January/February, 2006. [earlier version in *Proceedings, 32nd annual IEEE/ACM International Symposium on Computer Architecture*, Madison, Wisconsin, June, 2005] (with Onur Mutlu and Hyesoon Kim).

Wish Branches: Combining Conditional Branching and Predication for Adaptive Predicated Execution, *IEEE Micro*, Top Picks Special Issue, January/February, 2006. [earlier version in *Proceedings, 38th annual IEEE/ACM International Symposium on Microarchitecture*, Barcelona, November, 2005] (with Hyesoon Kim, Onur

Mutlu, and Jared Stark).

Runahead Execution: An Effective Alternative to Large Instruction Windows, *IEEE Micro,* Top Picks Special Issue, November/December, 2003. [earlier version in *Proceedings, 9th annual IEEE High Performance Computer Architecture Symposium.* Anaheim, CA, February, 2003] (with Onur Mutlu, Jared Stark, and Chris Wilkerson).

"New Requirements, Bottlenecks, and Good Fortune, Agents of Evolution of the Microprocessor," *Proceedings of the IEEE,* November, 2001.

"The First Computing Course for CS, CE, and EE Majors at Michigan," *The Interface* (a Newsletter published jointly by ASEE and the IEEE Education Society), November 1998, pp. 1-3.

"Identifying Obstacles in the Path to *More*," *IEEE Computer,* December 1997, Vol. 30, No. 12, p. 32.

"One billion transistors, one uniprocessor, one chip," *IEEE Computer,* September, 1997, (with Sanjay J. Patel, Marius Evers, Daniel H. Friendly, and Jared Stark).

"First, Let's Get the Uniprocessor Right," *Microprocessor Report*, (Invited article for 25th Anniversary of the Microprocessor Special Issue), August 5, 1996, pp. 23-24.

"The Microprocessor for Scientific Computing in the Year 2000," *IEEE Computational Science & Engineering,* Summer 1996, pp. 42-43.

"Education in Computer Science and Computer Engineering Starts with Computer Architecture," *Computer Architecture Technical Committee Newsletter,* June 1996.

"Scanning the Special Issue on Microprocessors," *Proceedings of the IEEE,* December 1995, Vol. 83, No. 12.

"The I/O Subsystem - A Candidate for Improvement," *IEEE Computer,* March 1994, Vol. 27, No. 3, pp. 15-16.

"Disk Arrays: High-Performance, High-Reliability Storage Subsystems," *IEEE Computer,* March 1994, Vol. 27, No. 3, pp. 30-36.

"Experimental Research in Computer Architecture," *IEEE Computer,* January 1991, Vol. 24, No. 1, pp. 14-16.

"Real Machines: Design Choices/Engineering Trade-Offs," *IEEE Computer,* January 1989, Vol. 22, No. 1, pp. 8-10.

RESEARCH PUBLICATIONS

Archival Journals:

Efficient Execution of Bursty Applications, *IEEE Computer Architecture Letters,* July, 2015, (with M Hashemi, D Marr, and D Carmean).

Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems, *ACM Transactions on Operating Systems,* April, 2012, (with Eiman Ebrahimi, Chang Joo Lee, and Onur Mutlu).

Prefetch-Aware Memory Controllers, *IEEE Transactions on Computers,* vol. 60, no. 10, October, 2011 (with Chang Joo Lee, Onur Mutlu, and Veynu Narasiman).

Virtual Program Counter (VPC) Prediction: Very Low-Cost Indirect Branch Prediction using Conditional Branch Prediction Hardware, *IEEE Transactions on Computers,* vol. 58, no. 9, September 2009 (with Hyesoon Kim, Jose Joao, Onur Mutlu, Chang Joo Lee, and Robert Cohn).

Dynamic Predication of Indirect Jumps, *IEEE Computer Architecture Letters,* vol. 7, June, 2008 (with Jose A. Joao, Onur Mutlu, and Hyesoon Kim).

Address-Value Delta (AVD) Prediction: A Hardware Technique for Efficiently Parallelizing Dependent Cache Misses, *IEEE Transacctions on Computers,* vol. 55, no. 12, December, 2006, (with Onur Mutlu and Hyesoon Kim).

An Analysis of the Performance Impact of Wrong-Path Memory References on Out-of-Order and Runahead Execution Processors, *IEEE Transactions on Computers,* vol. 54, no. 12, December, 2005, (with Onur Mutlu, Hyesoon Kim, and David Armstrong).

Using the First-Level Caches as Filters to Reduce the Pollution Caused by Speculative Memory References, *International Journal of Parallel Programming,* 2005, (with Onur Mutlu, Hyesoon Kim, and David N. Armstrong).

On Reusing the Results of Pre-Executed Instructions in a Runahead Execution Processor, *Computer Architecture Letters,* vol 4, no. 1, Jan. 2005 (with O. Mutlu, H. Kim, and J. Stark).

Soft Updates: A Solution to the Metadata Update Problem in File Systems, *ACM Transactions on Computer Systems,* vol. 18, no. 2, May 2000, pp 127-153 (with Greg Ganger, Marshall Kirk McKusick, and Craig A.N. Soules).

Evaluation of Design Options for the Trace Cache Fetch Mechanism, *IEEE Transactions on Computers,* February, 1999, (with Sanjay Patel and Daniel Friendly).

Increasing the Instruction Fetch Rate via Block-structured Instruction Set Architectures, *International Journal of Parallel Programming,* vol.26, no.4, August, 1998 (with E. Hao, P-Y Chang, M. Evers).

Using System Level Models to Evaluate I/O Subsystem Designs, *IEEE Transactions on Computers,* vol 47, no. 6 (June, 1998) (with Gregory Ganger).

Improving Branch Prediction Accuracy by Reducing Pattern History Table Interference, *International Journal of Parallel Programming,* 1997, vol 25, num 5 (with P-Y Chang and Marius Evers).

The Effects of Mispredicted-Path Execution on Branch Prediction Structures, *International Journal of Parallel Programming,* 1997, vol 25, num 5, pp. 363-384 (with Stephan Jourdan, Tse-Hao Hsing and Jared Stark).

Using Predicated Execution to Improve the Performance of a Dynamically Scheduled Machine with Speculative Execution, *International Journal of Parallel Programming,* vol.24, 1996 (with P-Y Chang, E. Hao, and P. Chang).

Branch Classification: A New Mechanism for Improving Branch Predictor Performance, *International Journal of Parallel Programming,* vol.24, 1996 (with Po-Yung Chang, Eric Hao, and Tse-Yu Yeh).

Enhancing Instruction Scheduling With a Block-Structured ISA, *International Journal of Parallel Programming,* vol. 23, no. 3, 1995 (with Stephen Melvin).

Report of the Purdue Workshop on Grand Challenges in Computer Architecture for the Support of High Performance Computing, *Journal of Parallel and Distributed Computing,* vol.16, pp. 199-211, 1992 (with 19 co-authors).

An Experimental Single-Chip Data Flow CPU, *IEEE Journal of Solid State Circuits,* January, 1992 (with G.Uvieghara, W. Hwu, Y. Nakagome, D. Jeong, D. Lee, D. Hodges).

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Checkpoint Repair for High Performance Out-of-Order Execution Machines, *IEEE Transactions on Computers,* December, 1987, (with Wen-mei Hwu).

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