Fall 2019 Course Syllabus*:
EE 440/396K Integrated Circuit Nanomanufacturing Techniques/ULSI Fabrication Techniques

Class: E E 396K 8-ULSI FABRICATION TECHNIQUES – 16815
E E 440 INTEG CIRC NANOMANUFAC TECHNIQS -16305
Fall 2019, M-W 10:30-12:00, ECJ 1.314

Labs: EER 0.766, and FNT 4.106: 3hrs/week lab times to be arranged via survey

Instructor: Praveen Pasupathy, MER 1.608B, phone 475-8285 e-mail: praveen@engr.utexas.edu
Web site: primarily Canvas, http://canvas.utexas.edu/
Office Hours: Mon, Wed 12:00-1:00; in EER 5.808 (tentative, will update if it changes) other times by arrangement; make sure to check in which office/campus I will be located.
Prerequisites: EE 339 Introduction to Electron Devices or equivalent

Objectives: The purpose of this course is to provide students with technical background and hands-on laboratory experience in silicon device fabrication. The course involves approximately three hours of lecture and three hours of laboratory per week for one semester. The following is an outline of subjects to be discussed and experiments to be performed in the laboratory.

Lecture:

- Semiconductor review and survey of IC processing.
- Silicon crystal growth and wafer preparation.
- Oxidation.
- Doping techniques: diffusion, ion implantation.
- Deposited thin films: polysilicon, silicon dioxide, silicon nitride, metals, silicides.
- Metallization and contacts.
- Epitaxial growth.
- Lithography: optical, electron beam, X-ray.
- Etching techniques: wet chemical, dry plasma.
- Yield considerations and contamination.

Laboratory:

Fabrication and testing of diffused resistors and MOS devices. In these experiments masks will be used containing arrays of the various discrete devices.
A. Photolithography.
B. Predep and drive.
C. Gate Oxide Growth.
D. Contact deposition and annealing.
E. Junction depth and sheet resistance measurements.
F. I-V and breakdown measurements.
G. MOS capacitor testing.
H. MOSFET testing.
I. Resistor testing.

Text Book: J. Plummer, M. Deal, and P. Griffin, **Silicon VLSI Technology**. This particular book is **NOT REQUIRED**, but you will need some reference text on semiconductor fabrication. Any of the one's listed below are also excellent:

FUNDAMENTALS OF SEMICONDUCTOR FABRICATION, Gary May and S. M. Sze.
S. A. Campbell, **The Science and Engineering of Microelectronic Fabrication**
S.K. Ghandhi, **VLSI Fabrication Principles**
editor S.M. Sze, **VLSI Technology**
S.Wolf & R.N Tauber , **SILICON PROCESSING FOR THE VLSI ERA: Volume 1 - Process Technology**
A. S. Grove, **Physics and Technology of Semiconductor Devices**, January 15, 1967, ISBN-10: 0471329983, ISBN-13: 978-0471329985

Copies of the viewgraphs (slides) I use in class will be available via our class home page on Blackboard/Canvas.
Other useful references:

Device Electronics for Integrated Circuits by R.S. Muller and T.I. Kamins**; MOS Physics and Technology** by E.H. Nicollian and J.R. Brews; **Physics of Semiconductor Devices** ed. S. Sze, **Solid State Electronic Devices**, Streetman and Banerjee.

Laboratory Manual: This course has a substantial laboratory component. Links to the material you need to download will be on-line through Canvas. The manual contains essential information on the laboratory, lab procedures, and work required for your lab grade. **We are updating various parts, and we will let you know which sections to OBTAIN A COPY OF AS SOON AS POSSIBLE.** As new materials become available, I will notify you.

Laboratory Reports: THE CURRENT PROCEDURE IS: instead of widely time spaced "big" reports (as was done in the past) you will instead, do shorter WEEKLY lab write-ups. **DETAILS WILL BE DISTRIBUTED IN A SEPARATE DOCUMENT.**

Grades

Your grades will be based upon performance in lab, weekly lab write-ups, and exams. I will post example problem sets, along with solutions, but there is no graded homework. **However, I strongly recommend you work the sample problems and read the solutions!!!** Details of work expected in conjunction with lab are given in the lab manual and will also be distributed in a separate document.

EE 440 weighting for different assignments:

Exam I	23%
Exam II	23%
Lab grade	24%
Final	30%
	100%

EE 396K weighting for different assignments:

Exam I	22%
Exam II	22%
Lab grade	20%
Term Paper	6%
Final	30%
	100%

The worst-case grades will be based on (final total points earned, rounded to tenth):

A	100-90.1%				
B+	86.6-90.0	B	82.5-86.5	B-	80.0-82.4
C+	76.6-79.9	C	73.0-76.5	C-	70.0-72.9
D+	65.0-69.9	D	60.0-64.9	D-	55.1-59.9
F	0-55.0%				

Special Note to EE396K students:

Since you are enrolled for graduate credit, I will expect you to do more than the undergraduates. This will take the form of a term lab project or a term review paper (approximately ~4 type-written pages long) on a topic related to device fabrication or processing. **You must pick a topic and clear it with me by Fri., Oct. 11.** The paper should review **current** work in the literature related to your topic. It is due on Mon., Dec. 09, 2019. More details to follow. The project/paper grade will be factored into your lab grade. I will provide further instructions in a separate document.

FINAL (to the best of my current knowledge and understanding):

From the course schedule https://registrar.utexas.edu/schedules/199/finals :

"If the beginning time of the class is ***exactly halfway*** between two standard class beginning times, the class ***defaults to the later time***. For example:

- WF 2:30 pm–4:00 pm classes default to the same exam time as MWF 3:00 pm–4:00 pm classes.
- TTH 1:15 pm-2:45 pm classes default to the same exam time as TTH 2:00 pm-3:30 pm classes."

– Based on this we belong to MWF 11am -12 pm meeting times, and for that class time listed 'Index of (default) final exam times' is **Monday, December 16, 2:00 pm-5:00 pm**

Policy on CHEATING: University of Texas at Austin Honor Code: http://catalog.utexas.edu/general-information/the-university/#universitycodeofconduct

You are expected to do your own work at ALL times. I expect discuss of assignments, but you MUST do your own ORIGINAL written work. Any evidence of cheating or plagiarism* will be reported to the dean of students, and I will recommend the penalty be FAILURE in the class.

***PLAGIARISM**

You may or may not have had an opportunity to learn about what constitutes plagiarism. You are REQUIRED to complete this module (link below) on plagiarism for this course. This will be of broader benefit to you in all your endevours. Feel free to ask and /or clarify if you have questions before you submit your work.

HTTP://GUIDES.LIB.UTEXAS.EDU/C.PHP?G=700523&P=5070724

The following is extracted from the document "On Being A Scientist: Responsible Conduct In Research" by the COMMITTEE ON SCIENCE, ENG, NATIONAL ACADEMY OF ENGINEERING, INSTITUTE OF MEDICINE, NATIONAL ACADEMY PRESS, Washington, D.C. 1995.

THIS BOOK SEEMS TO BE AVAILABLE ON LINE (for a while it was not); try here:

http://www.nap.edu/openbook.php?record_id=4917

THE UNIVERSITY OF TEXAS AT AUSTIN PROVIDES UPON REQUEST APPROPRIATE ACADEMIC ADJUSTMENTS FOR QUALIFIED STUDENTS WITH DISABILITIES. FOR MORE INFORMATION, CONTACT THE OFFICE OF THE DEAN OF STUDENTS AT 471-6259. PLEASE SEE HTTP://DIVERSITY.UTEXAS.EDU/DISABILITY/

OFFICIAL UNIVERSITY CALENDAR AVAILABLE AT: https://registrar.utexas.edu/calendars/19-20

Notice of planned absences for the observance of religious holy days: BY UT AUSTIN POLICY, YOU MUST NOTIFY ME OF YOUR PENDING ABSENCE AT LEAST FOURTEEN DAYS PRIOR TO THE DATE OF OBSERVANCE OF A RELIGIOUS HOLY DAY. IF YOU MUST MISS A CLASS, AN EXAMINATION, A WORK ASSIGNMENT, OR A PROJECT IN ORDER TO OBSERVE A RELIGIOUS HOLY DAY, YOU WILL BE GIVEN AN OPPORTUNITY TO COMPLETE THE MISSED WORK WITHIN A REASONABLE TIME AFTER THE ABSENCE. (See http://catalog.utexas.edu/general-information/academic-policies-and-procedures/attendance/)

Course Evaluation: University survey during last week of class.

Emergency preparedness: see http://www.utexas.edu/safety/preparedness/, http://www.utexas.edu/safety/preparedness/terms/emergency_terms.pdf and http://www.utexas.edu/emergency/

Classroom Evacuation for Students

All occupants of university buildings are required to evacuate a building when a fire alarm and/ or an official announcement is made indicating a potentially dangerous situation within the building.

Familiarize yourself with all exit doors of each classroom and building you may occupy. Remember that the nearest exit door may not be the one you used when entering the building.

If you require assistance in evacuation, inform your instructor in writing during the first week of class.

For evacuation in your classroom or building:

1. Follow the instructions of faculty and teaching staff.
2. Exit in an orderly fashion and assemble outside.
3. Do not re-enter a building unless given instructions by emergency personnel.

Concealed carry of firearms ("campus carry"):

https://campuscarry.utexas.edu/
https://campuscarry.utexas.edu/students
https://campuscarry.utexas.edu/faculty

Readings should be completed BEFORE class (subject to revision based on instruction).

Lecture	Date	Topic	Plummer, Deal, & Griffin (by ch & sect)
1	8/28	Introduction, history	
2	9/4	review of semiconductors, CMOS Process Overview	
3	9/9	scaling; Crystal structure,	Ch 1-2
4	9/11	Crystal structure, Impurities; defects	3.1-3.2, 3.2.4, 3.5.1
5	9/16	Impurities; defects, Crystal growth; segregation/distribution effects; gettering, oxygen in Si	3.2.2, 3.5.5
6	9/18	gettering, oxygen in Si; intro to oxidation, Basic oxidation processes, Oxidation kinetics, thin oxide	6.1-6.5.1, 6.6
7	9/23	Basic oxidation processes, Oxidation kinetics, doping effects;	7.1-7.2.3, 7.5.2-7.5.3
8	9/25	doping effects, mobile charge, EOT	7.2.4-7.2.9
9	9/30	Diffusion, Fick's laws;	8.1-8.3; 8.5
10	10/2	Vacancy-Impurity interactions; diffusion profiles [**Graduate Student paper topics due Oct 11]**	
11	10/7	diffusion profiles; boron & phosphorus diffusion	
12	10/9	boron & phosphorus diffusion; Ion implantation up to projected range	
13	10/14	boron & phosphorus diffusion Implantation: channeling, damage	7.4; 8.4
14	10/16	**EXAM I (material up to/including DIFFUSION)**	9.1
15	10/21	Ion implantation projected range, channeling; Implant systems, applications; evaluation techniques	
16	10/23	Implant damage, systems, applications; evaluation techniques , evaluation of doped layers, Irvin curves,	9.2, 9.3
17	10/28	evaluation techniques , evaluation of doped layers, Hall effect, SIMS, kinetic gas theory, C-V	
18	10/30	Irvin curves, Hall effect, SIMS step coverage, physical vapor deposition, thermal evaporation, sputtering; Chemical Vapor Deposition	11.1, 11.2
19	11/4	step coverage, physical vapor deposition poly, oxide, Reflow, Nitride, intro to epi, rest of epi on narrated on-line lecture (Epitaxy; autodoping, pattern shift);	11.3; 5.1, 5.2, 5.3
20	11/6	physical vapor deposition, basic CVD; (poly, oxide, Reflow, Nitride material details via on-line narrated lecture); (intro to epi, rest of epi on narrated on-line lecture: Epitaxy; autodoping, pattern shift); Metallization, stress, intermetallic compounds,	
21	11/11	intermetallic compounds; intro to Lithographys	
22	11/13	**EXAM II (ion implant through metals to Kirkendal)**	
23	11/18	electromigration, CMP, intro to Lithographys Lithography, optical transfer, masks; resists	
24	11/20	Masks, resists, aligners; Intro to etch, bias	10.1, 10.2.1
25	11/25	aligners; Intro to etch etch selectivity, wet etching	
26	12/2	etch selectivity, wet etching (via narration) Etching: bias & selectivity, wet etching	10.2.2, 10.3
27	12/4	Plasma etching	
28	12/9	catch up / class survey; LAST CLASS	