The University of Texas at Austin
Department of Electrical and Computer Engineering

EE 382M.7, VLSI I (Unique numbers 16675, 16680, 16685, 16690, 16694)

EE 460R, Introduction to VLSI Design (Unique numbers 16460, 16464)

Class meets Tu. Th. 12:30 - 2:00 pm, EER 1.518

INSTRUCTOR:

Jacob A. Abraham
Office: EER 4.874, Phone: (512) 471-8983
Office hours: Tu. Th. 11:00 - 12:30, in EER 4.702, or by appointment
E-mail: *jaa at cerc.utexas.edu*

ADDITIONAL DISCUSSION HOURS:
Some Sundays, 1:00pm - 3:00pm, to be announced.

Textbook: **CMOS VLSI Design** by Weste and Harris, 4th edition, Addison-Wesley/Pearson, 2011.

PREREQUISITES:

Logic design, computer architecture.

Students are expected to be able to design logic circuits and implement state machines using logic and memory elements, and have an understanding of computer architecture.

OUTLINE:

This course covers all the aspects of design and synthesis of Very Large Scale Integrated (VLSI) chips using CMOS technology. Complex digital systems are built using integrated circuit cells as building blocks and employing hierarchical design methods. Design issues at layout, schematic, logic and RTL levels will be studied. Commercial design software will be used for laboratory exercises.

The lectures will discuss the basics of digital CMOS design. Homework problems will be assigned to reinforce the concepts discussed in class. Students are encouraged to work together on the homework problems, and may turn in a single solution as a team. However, every member of the team should make sure he or she thoroughly understands the problems, since this will help in the exams. **Homework is due week after it is assigned and should be uploaded on to Canvas (please remember to note the names of all the team participants on the submission)**.

Application of the concepts studied in class to larger designs will be done via the computer-aided design laboratory exercises which are based on common industry design practice. Commercial tools and an open-source standard cell library are used for the labs. Laboratory exercises will enable students to learn all aspects of digital design, including: layout of simple cells and the generation of larger blocks using these cells; designs at the schematic level, and the use of timing verification tools; the use of automatic place-and-route tools, and the concepts of post-

layout timing closure; design at the register-transfer level using the Verilog hardware description language; and the use of synthesis tools to generate the design details with a standard cell library.

There will be two in-class exams. All exams are open book and open notes. Several previous exams will be posted before the exam dates. The final exam for EE 460R will be on the date and location assigned by the registrar (see final exam schedule available about a month before the end of the semester). There is no final exam for graduate students; the team project replaces the final exam. Graduate students are also required to do a team project and submit the design details and results along with a summary report. The teams should work with the instructor and the TAs throughout the semester on the project.

TEACHING ASSISTANTS

There are two teaching assistants for the class. They will help you learn the tools needed to complete the laboratory exercises and gain further understanding of the topics in the class.

Hyunsu Chae, *hyunsu.chae at utexas.edu*

Ling Lin, *linling at gmail.com*

Sunny Bhagia, *sunnysb at utexas.edu*

Lab./discussion: EER 0.810.
Time slots:
W. 6:00 - 9:00 pm
Th. 3:30 - 6:30 pm
Th. 6:30 - 9:30 pm
F. 12:00 pm - 3:00 pm
F. 3:00 p.m. - 6:00 pm

Piazza discussion forum

LABORATORY: The laboratory exercises are key to understanding to designing VLSI circuits in real life. Unfortunately, the commercial tools we use are very complicated and require a steep learning curve to complete the laboratory exercises by the deadlines. The TAs will hold demonstrations and discussion sessions in EER 0.810, to help students learn the tools rapidly. Each student is enrolled in a specific lab session, but students are welcome to attend any session of their choice; however, please let the TAs know that you have changed the session you are attending.

Since it is very important to meet schedules in the real world, we will add/subract points for the labs based on whether the submission is early or late.
Early submission: additional 5% points per day, maximum of 10%.
Late submission: loss of 5% per day, maximum of 25%; submissions will not be accepted more than 5 days late.

DESIGN PROJECT

Graduate students are required to design a VLSI subsystem as part of a team; this is in lieu of a final exam. The link above provides more information.

Course Outline and Schedule (tentative)

DATE	DAY	TOPIC OF LECTURE/DISCUSSION	Reading	HOMEWORK	LAB. ASSIGNMENT	EXAMS
Aug. 29	Thur.	1. Introduction, CMOS Transistors	1.1 - 1.3	Homework 0	**Lab. 1 Assigned**	
Sep. 3	Tue.	2. CMOS Fabrication and Layout	3.1 - 3.5			
Sep. 5	Thur.	3. Implementing Logic in CMOS	1.4 - 1.5	Homework 1		
Sep. 10	Tue.	4. MOS Transistor Theory	2.1 - 2.3.1			
Sep. 12	Thur.	5. CMOS Gate Characteristics	2.3.2 - 2.6, 4.3 - 4.4	Homework 2		
Sep. 17	Tue.	6. Logical Effort	4.3 - 4.5			
Sep. 19	Thur.	7. Combinational Circuits	9.2 - 9.2.1	Homework 3		
Sep. 24	Tue.	8. Design of Adders	11.1 - 11.2		**EE 382M: Lab. 1 Due/Lab. 2 Assigned**	
Sep. 26	Thur.	9. Datapath Design	11.3 - 11.10			
Oct. 1	Tue.	10. Interconnects in CMOS Technology	10.1 - 10.4			
Oct. 3	Thur.					Exam. 1
Oct. 8	Tue.	11. Sequential Elements	6.1 - 6.6	Homework 4	**EE 460R: Lab. 1 Due/Lab. 2 Assigned**	
Oct. 10	Thur.	12. Dynamic CMOS Logic	9.2.2 - 9.2.5, 9.4 - 9.5			
Oct. 15	Tue.	13. Memories	12.1 - 12.3	Homework 5		
Oct. 17	Thur.	14. Introduction to Verilog	Appendix A		**EE 382M: Lab. 2 Due/Lab. 3 Assigned**	
Oct. 22	Tue.	15. CAMs, ROMs, PLAs	12.4 - 12.7	Homework 6		

Oct. 24	Thur.	16. Deep Submicron Issues	2.4, 7.2			
Oct. 29	Tue.	17. Circuit Design Pitfalls	7.3, 9.3	Homework 7		
Oct. 31	Thur.	18. Design Verification	15.1 - 15.4			
Nov. 5	Tue.	19. Design for Low Power	3.1 - 3.5	Homework 8	**EE 460R: Lab. 2 Due/Lab. 3 Assigned**	
Nov. 7	Thur.	20. Introduction to Manufacturing Test	15.5, Notes			
Nov. 12	Tue.	21. Introduction to Design for Test	15.6, Notes		**EE 382M: Lab. 3 Due**	
Nov. 14	Thur.					Exam. 2
Nov. 19	Tue.	22. Introduction to Formal Verification	Notes	Homework 9		
Nov. 21	Thur.	23. Skew-Tolerant Design	10.2.4 - 10.2.5, 10.5 - 10.9			
Nov. 26	Tue.	24. Scaling, Economics,	7.4 - 7.6, 9.5 - 9.6, 14.5			
Dec. 3	Tue.	25. Packaging and I/O	13.2 - 13.8			
Dec. 5	Thur.	26. Future Directions	Notes		**EE 460R: Lab. 3 due (December 9)**	

GRADES:

EE 382M:

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Homework              10%
Exams I and II        30%
Laboratory Exercises  45%
Project               15%
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EE 460R:

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Homework              10%
Exams I and II        25%
Laboratory Exercises  45%
Final Exam            20%
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Allegations of Scholastic Dishonesty will be dealt with according to the UT Honor Code. Although we encourage you to study together, your designs and examinations you take MUST be your own work. Providing information to another student where prohibited, or obtaining information from another student where prohibited is considered cheating. This includes the exchange of any information during an examination and any part of your design for the laboratory exercises. Allowing another student to read something on your paper during an examination is considered cheating. In fact, leaving information unprotected so it can be compromised by another student is considered cheating. This includes sheets of paper lying about in your dorm room, and computer files that are not properly protected.

The University of Texas at Austin provides, upon request, appropriate academic adjustments for qualified students with disabilities. who may request appropriate academic accommodations from the Division of Diversity and Community Engagement, Services for Students with Disabilities, 512-471-6259, http://diversity.utexas.edu/disability/

By UT Austin policy, you must notify me of your pending absence at least fourteen days prior to the date of observance of a religious holy day. If you must miss a class, an examination, a work assignment, or a project in order to observe a religious holy day, you will be given an opportunity to complete the missed work within a reasonable time after the absence.

Classroom Evacuation for Students

All occupants of university buildings are required to evacuate a building when a fire alarm and/or an official announcement is made indicating a potentially dangerous situation within the building.

Familiarize yourself with all exit doors of each classroom and building you may occupy. Remember that the nearest exit door may not be the one you used when entering the building.

If you require assistance in evacuation, inform your instructor in writing during the first week of class.

For evacuation in your classroom or building:

1. Follow the instructions of faculty and teaching staff.
2. Exit in an orderly fashion and assemble outside.
3. Do not re-enter a building unless given instructions by emergency personnel.